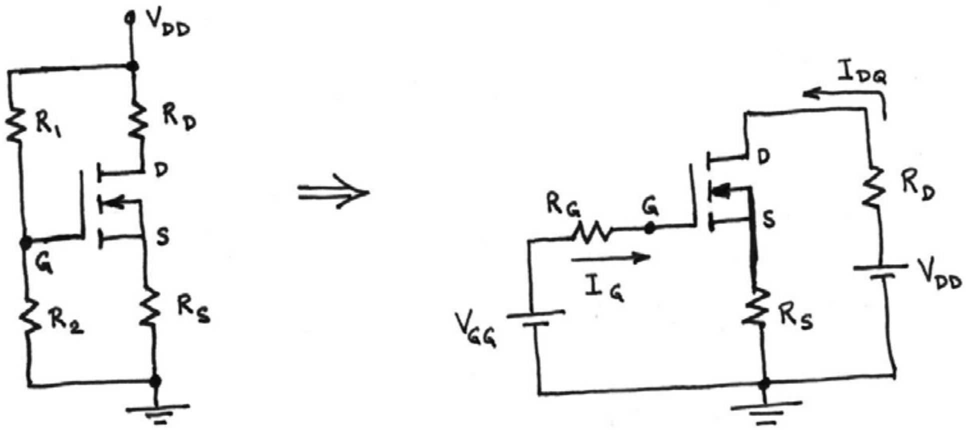
Solution #1

(a) DC analysis

Capacitors act as decoupling capacitors for DC signals.
Circuit reduces to:



$$V_{GG} = \frac{R_2}{R_1 + R_2} \cdot V_{DD} = \frac{1}{1+1} \cdot 10 = 5\,V$$

$$R_{GG} = \frac{R_1 R_2}{R_1 + R_2} = \frac{1 \times 1}{1+1} = 0.5\,M\Omega$$

$$V_{GG} - R_G I_G - V_{GSQ} - R_S I_{DQ} = 0$$

since $I_G = 0$ $\quad V_{GSQ} = V_{GG} - R_S I_{DQ} = 5 - 6 I_{DQ}$
(note I_{DQ} in mA)

since $i_D = K(V_{GS} - V_T)^2$

$$\therefore I_{DQ} = K(V_{GG} - R_S I_{DQ} - V_T)^2$$
$$= 0.5(5 - 6I_{DQ} - 1)^2 = 18 I_{DQ}^2 - 24 I_{DQ} + 8$$

$$\therefore 18 I_{DQ}^2 - 25 I_{DQ} + 8 = 0$$

$$I_{DQ} = \frac{25 \pm \sqrt{(25)^2 - 4 \times 18 \times 8}}{2 \times 18} = \frac{25 \pm 7}{36}$$

$I_{DQ} = 0.889\,mA$ or $0.5\,mA$

for $I_{DQ} = 0.889\,mA$ $V_{GSQ} = 5 - 6 \times 0.889 = -0.334\,V$

for $I_{DQ} = 0.5\,mA$ $V_{GSQ} = 5 - 6 \times 0.5 = 2\,V$

Since $V_{GS} \geq V_T = 1\,V$ for the FET to be ON

$\Rightarrow \therefore I_{DQ} = 0.5\,mA$ and $V_{GSQ} = 2\,V$

$$V_{DD} - R_D I_{DQ} - V_{DSQ} - R_S I_{DQ} = 0$$

$$V_{DSQ} = 10 - 6 \times 0.5 - 6 \times 0.5$$

$$\Rightarrow V_{DSQ} = 4\,V$$

(b) <u>DC Load Line</u>

$$i_D = \frac{V_{DD} - V_{DS}}{R_D + R_S}$$

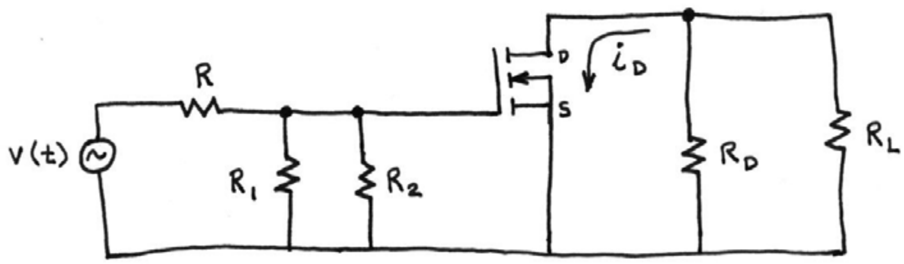
at $i_D = 0$ $V_{DS} = V_{DD} = 10\,V$

at $V_{DS} = 0$ $i_D = \frac{V_{DD}}{R_D + R_S} = \frac{10}{6+6} = 0.833\,mA$

(see figure)

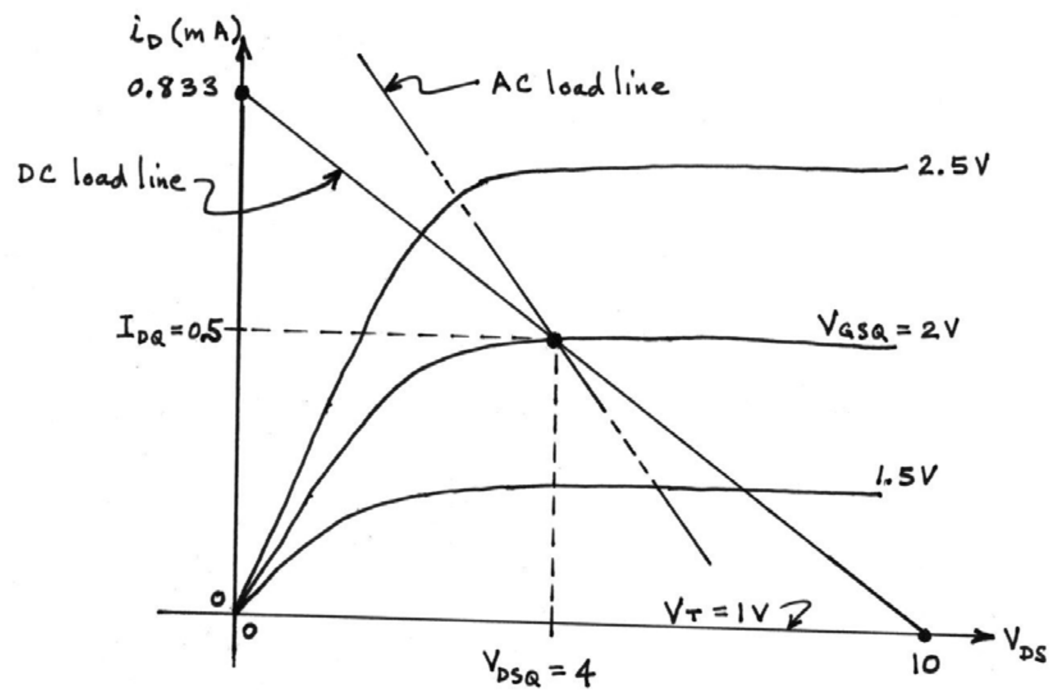
(c) AC analysis

Capacitors act as coupling capacitors to AC signals.
Short all DC supplies.
Circuit reduces to:



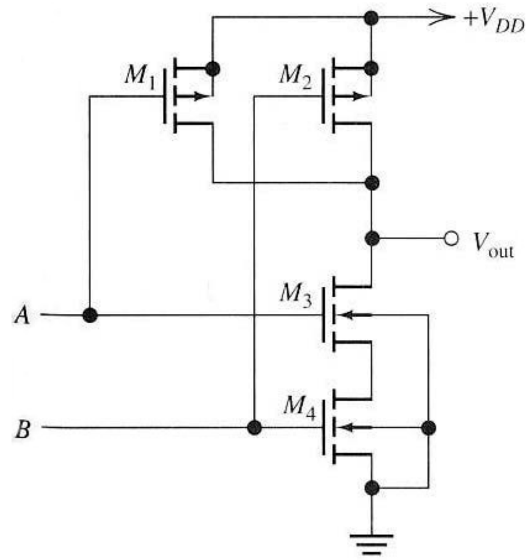
$$-(R_D /\!/ R_L)\, i_D - V_{DS} = 0$$

$$\frac{i_D}{V_{DS}} = -\frac{1}{\frac{R_D R_L}{R_D + R_L}} = -\frac{1}{\frac{6\times 12}{6+12}} = -\frac{1}{4k\Omega} \text{ (slope)}$$



Solution #2

A	B	M_1	M_2	M_3	M_4	V_{out}
1	1	**OFF**	**OFF**	**ON**	**ON**	**0**
1	0	**OFF**	**ON**	**ON**	**OFF**	**1**
0	1	**ON**	**OFF**	**OFF**	**ON**	**1**
0	0	**ON**	**ON**	**OFF**	**OFF**	**1**



The circuit is a CMOS NAND gate, where $V_{out} = \overline{A \cdot B}$

M_1 and M_2 are P-type enhancement MOSFET's.
To be ON, $V_{GS} \leq V_T$ (ie: $V_T = -1V$).

M_3 and M_4 are N-type enhancement MOSFET's.
To be ON, $V_{GS} \geq V_T$ (ie: $V_T = +1V$).
Note that the source and substrate for these two FET's are tied to reference (ie: ground).
Specifically, for M_3 to be ON, $V_{G\text{-}Substrate} \geq V_T$.

Solution #3

$V_i = 0$ and $i_i = 0$

$$i_1 = \frac{V_{in}}{R_1} \quad \ldots\ldots\ldots (1)$$

$$i_2 = i_1 \quad \ldots\ldots\ldots (2)$$

$$R_2 i_2 = R_3 i_3 \quad \ldots\ldots\ldots (3)$$

$$i_4 = i_2 + i_3 \quad \ldots\ldots\ldots (4)$$

$$V_o = -R_4 i_4 - R_3 i_3 \quad \ldots\ldots\ldots (5)$$

from (1) and (2) $\quad i_2 = \frac{V_{in}}{R_1} \quad \ldots\ldots\ldots (6)$

substitute into (3) $\quad i_3 = \frac{R_2}{R_1 R_3} \cdot V_{in} \quad \ldots (7)$

substitute (6) and (7) into (4)

$$i_4 = V_{in}\left(\frac{1}{R_1} + \frac{R_2}{R_1 R_3}\right) \quad \ldots\ldots\ldots (8)$$

substitute (7) and (8) into (5)

$$V_o = -V_{in}\left(\frac{R_2}{R_1} + \frac{R_4}{R_1} + \frac{R_2 R_4}{R_1 R_3}\right)$$

$$\therefore \frac{V_o}{V_{in}} = -\left(\frac{R_2}{R_1} + \frac{R_4}{R_1} + \frac{R_2 R_4}{R_1 R_3}\right)$$