Université d'Ottawa
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CEG2536 Architecture des ordinateurs I

University of Ottawa
Faculty of Engineering
School of Electrical Engineering
and Computer Science
CEG2136 Computer Architecture I

Quiz 3 / Fall 2011

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Even

Q1. The content of a memory fragment of the Basic Computer is given below:

Address	Content
072B	DADA
072C	172B
072D	3019

The Basic Computer follows to fetch instruction from address 072C. Fill out the following table with the values of the corresponding registers at the end of every clock cycle (T_0, T_1, T_2) during this fetch phase.

Write a "*" if the register content is unknown.

	PC	AR	IR	RTL; comments
T_0	072C	72C	*	AR <- PC
T_1	072D	72C	172B	IR <- M[0F1A], PC <- PC+1
T_2	072D	72B	172B	AR <- IR[11..0], D_0 … D_7 <- IR[11..0], I <- IR[15]
	2 x 0.5 pts	3 x 0.5 pts	3 x 0.5 pts	3 x s

Q2. Scan the table of microoperations of the Basic Computer on the next page to find all the RTL statements that change the content of register SC:

a) Write down the RTL statements which you found above that change the SC content

RT_2:	*PC <- PC+1, IEN <- 0, R <- 0,* ***SC <- 0***
D_0T_5:	*AC <- AC ^ DR,* ***SC <- 0***
D_1T_5:	*AC <- AC + DR, E <-* C_{out}*,* ***SC <- 0***
D_2T_5:	*AC <- DR,* ***SC <- 0***
D_3T_4:	*M[AR] <- AC,* ***SC <- 0***
D_4T_4:	*PC <- AR,* ***SC <- 0***
D_5T_5:	*PC <- AR,* ***SC <- 0***
D_6T_6DR':	*if (DR = 0) then (PC <- PC + 1),* ***SC <- 0***
$D_7I'T_3 = r$	**SC <- 0**

b) Derive the Boolean expression of the SC control functions (e.g., CLR_{SC}).

$CLR_{SC} =$

$RT_2+D_0T_5+D_1T_5+D_2T_5+D_3T_4+D_4T_4+D_5T_5+D_6T_6DR'+D_7I'T_3 =$

$= RT_2 + D_7I'T_3 + (D_3+ D_4)\,T_4 + (D_0 + D_1 + D_2 + D_5)T_5 + D_6T_6DR'$

Q3. Scan the table of microoperations of the Basic Computer on the next page to find all the RTL statements whose microoperations change the state of flip-flop *IEN*.

a. Write down the RTL statements which you found above that change the *IEN* state.

RT_2:	*PC <- PC+1, IEN <- 0, R <- 0, SC <- 0*
$pB_7 = D_7IT_3\,B_7$:	*IEN <- 1*
$pB_6 = D_7IT_3\,B_6$:	*IEN <- 0*

b) Derive the Boolean expression of the control of the *IEN* flip-flop, assuming that it has to be implemented with a *JK* flip-flop.

$J_{IEN} = D_7IT_3\,B_7$

$K_{IEN} = D_7IT_3\,B + RT_2$

					S_{IEN}	R_{IEN}	CLR_{SC}
Fetch	$R'T_0$:						
	$R'T_1$:						
Decode	$R'T_2$:						
Indirect	D'_7IT_3:	$AR \leftarrow M[AR]$					
Interrupt:							
	$T_0'T_1'T_2'(IEN)(FGI + FGO)$:	$R \leftarrow 1$					
	RT_0:	$AR \leftarrow 0, TR \leftarrow PC$					
	RT_1:	$M[AR] \leftarrow TR, PC \leftarrow 0$					
	RT_2:	$PC \leftarrow PC+1$, $IEN \leftarrow 0$, $R \leftarrow 0$, $SC \leftarrow 0$				1	1
Memory-reference:							
AND	D_0T_4:	$DR \leftarrow M[AR]$					
	D_0T_5:	$AC \leftarrow AC \wedge DR$, $SC \leftarrow 0$					1
ADD	D_1T_4:	$DR \leftarrow M[AR]$					
	D_1T_5:	$AC \leftarrow AC + DR, E \leftarrow C_{out}$, $SC \leftarrow 0$					1
LDA	D_2T_4:	$DR \leftarrow M[AR]$					
	D_2T_5:	$AC \leftarrow DR$, $SC \leftarrow 0$					1
STA.	D_3T_4:	$M[AR] \leftarrow AC$, $SC \leftarrow 0$					1
BUN	D_4T_4:	$PC \leftarrow AR$, $SC \leftarrow 0$					1
BSA	D_5T_4:	$M[AR] \leftarrow PC, AR \leftarrow AR + 1$					
	D_5T_5:	$PC \leftarrow AR$, $SC \leftarrow 0$					1
ISZ	D_6T_4:	$DR \leftarrow M[AR]$					
	D_6T_5:	$DR \leftarrow DR + 1$					
	D_6T_6:	$M[AR] \leftarrow DR$,					
	D_6T_6DR':	if $(DR = 0)$ then $(PC \leftarrow PC + 1)$, $SC \leftarrow 0$					1
Register-reference:							
	$D_7I'T_3 = r$	(common to all register-reference instructions)					
	$IR(i) = B_i$	(i = 0, 1, 2, ... , 11)					
	r:	$SC \leftarrow 0$					1
CLA	rB_{11}:	$AC \leftarrow 0$					(1)
CLE	rB_{10}:	$E \leftarrow 0$					(1)
CMA	rB_9:	$AC \leftarrow AC'$					(1)
CME	rB_8:	$E \leftarrow E'$					(1)
CIR	rB_7:	$AC \leftarrow shr\ AC, AC(15) \leftarrow E, E \leftarrow AC(0)$					(1)
CIL	rB_6:	$AC \leftarrow shlAC, AC(0) \leftarrow E, E \leftarrow AC(15)$					(1)
INC	rB_5:	$AC \leftarrow AC + 1$					(1)
SPA	$rB_4AC'(15)$:	If $(AC(15) = 0)$ then $(PC \leftarrow PC + 1)$					(1)
SNA	$rB_3AC(15)$:	If $(AC(15) = 1)$ then $(PC \leftarrow PC + 1)$					(1)
SZA	rB_2AC':	If $(AC = 0)$ then $(PC \leftarrow PC + 1)$					(1)
SZE	rB_1E':	If $(E = 0)$ then $(PC \leftarrow PC + 1)$					(1)
HLT	rB_0:	$S \leftarrow 0$					(1)
Input-output:							
	$D_7IT_3 = p$	(common to all input-output instructions)					
	$IR(i) = B_i$	(i = 6, 7, 8, 9, 10, 11)					
	p:	$SC \leftarrow 0$					
INP	pB_{11}:	$AC(0\text{-}7) \leftarrow INPR$, $FGI \leftarrow 0$					
OUT	pB_{10}:	$OUTR \leftarrow AC(0\text{-}7)$, $FGO \leftarrow 0$					
SKI	pB_9FGI:	If $(FGI = 1)$ then $(PC \leftarrow PC + 1)$					
SKO	pB_8FGO:	If $(FGO = 1)$ then $(PC \leftarrow PC + 1)$					
ION	pB_7:	$IEN \leftarrow 1$			1		
IOF	pB_6:	$IEN \leftarrow 0$				1	

No needed (being redundant), but acceptable

Odd

Q1. The content of a memory fragment of the Basic Computer is given below:

Address	Content
0F19	FFFF
0F1A	2F19
0F1B	3019

The Basic Computer follows to fetch instruction from address 0F1A. Fill out the following table with the values of the corresponding registers at the end of every clock cycle (T_0, T_1, T_2) during this fetch phase.

Write a "*" if the register content is unknown.

	PC	AR	IR	RTL; comments
T_0	0F1A	(0)F1A	*	AR <- PC
T_1	(0)F1B	(0)F1A	2F19	IR <- M[0F1A], PC <- PC+1
T_2	(0)F1B	(0)F19	2F19	AR <- IR[11..0], D_0 … D_7 <- IR[11..0], I <- IR[15]

Q2. Scan the table of microoperations of the Basic Computer on the next page to find all the RTL statements that change the content of register DR.

a) Write down the RTL statements which you found above that change the DR content

D_0T_4: DR <- M[AR]
D_1T_4: DR <- M[AR]
D_2T_4: DR <- M[AR]
D_6T_4: DR <- M[AR]
D_6T_5: DR <- DR + 1

b) Derive the Boolean expression of the DR control functions (e.g., LD_{DR} and INR_{DR}).

$LD_{DR} = D_0T_4 + D_1T_4 + D_2T_4 + D_6T_4$

$INR_{DR} = D_6T_5$

Q3. Scan the table of microoperations of the Basic Computer on the next page to find all the RTL statements whose microoperations change the state of flip-flop *R*.

b. Write down the RTL statements which you found above that change the R state.

$T_0'T_1'T_2'(IEN)(FGI + FGO)$: **R <- 1**
RT_2: PC <- PC+1, IEN <- 0, **R <- 0,** SC <- 0

c. Derive the Boolean expression of the control of the *R* flip-flop, assuming that it has to be implemented with a *JK* flip-flop.

$J_R = T_0'T_1'T_2'(IEN)(FGI + FGO)$: $K_R = RT_2$

			LD_{DR}	INR_{DR}	S_R	R_R	
Fetch	$R'T_0$:						
	$R'T_1$:						
Decode	$R'T_2$:						
Indirect	D'_7IT_3:	$AR \leftarrow M[AR]$					
Interrupt:							
$T_0'T_1'T_2'(IEN)(FGI + FGO)$:		$R \leftarrow 1$			1		
	RT_o:	$AR \leftarrow 0, TR \leftarrow PC$					
	RT_1:	$M[AR] \leftarrow TR, PC \leftarrow 0$					
	RT_2:	$PC \leftarrow PC+1, IEN \leftarrow 0, R \leftarrow 0, SC \leftarrow 0$				1	
Memory-reference:							
AND	D_0T_4:	$DR \leftarrow M[AR]$	1				
	D_0T_5:	$AC \leftarrow AC \wedge DR, SC \leftarrow 0$					
ADD	D_1T_4:	$DR \leftarrow M[AR]$	1				
	D_1T_5:	$AC \leftarrow AC + DR, E \leftarrow C_{out}, SC \leftarrow 0$					
LDA	D_2T_4:	$DR \leftarrow M[AR]$	1				
	D_2T_5:	$AC \leftarrow DR, SC \leftarrow 0$					
STA.	D_3T_4:	$M[AR] \leftarrow AC, SC \leftarrow 0$					
BUN	D_4T_4:	$PC \leftarrow AR, SC \leftarrow 0$					
BSA	D_5T_4:	$M[AR] \leftarrow PC, AR \leftarrow AR + 1$					
	D_5T_5:	$PC \leftarrow AR, SC \leftarrow 0$					
ISZ	D_6T_4:	$DR \leftarrow M[AR]$	1				
	D_6T_5:	$DR \leftarrow DR + 1$		1			
	D_6T_6:	$M[AR] \leftarrow DR,$					
	D_6T_6DR':	$if (DR = 0) then (PC \leftarrow PC + 1), SC \leftarrow 0$					
Register-reference:							
	$D_7I'T_3 = r$	(common to all register-reference instructions)					
	$IR(i) = B_i$	(i = 0, 1, 2, ... , 11)					
	r:	$SC \leftarrow 0$					
CLA	rB_{11}:	$AC \leftarrow 0$					
CLE	rB_{10}:	$E \leftarrow 0$					
CMA	rB_9:	$AC \leftarrow AC'$					
CME	rB_8:	$E \leftarrow E'$					
CIR	rB_7:	$AC \leftarrow shr\ AC, AC(15) \leftarrow E, E \leftarrow AC(0)$					
CIL	rB_6:	$AC \leftarrow shlAC, AC(0) \leftarrow E, E \leftarrow AC(15)$					
INC	rB_5:	$AC \leftarrow AC + 1$					
SPA	$rB_4AC'(15)$:	$If (AC(15) = 0) then (PC \leftarrow PC + 1)$					
SNA	$rB_3AC(15)$:	$If (AC(15) = 1) then (PC \leftarrow PC + 1)$					
SZA	rB_2AC':	$If (AC = 0) then (PC \leftarrow PC + 1)$					
SZE	rB_1E':	$If (E = 0) then (PC \leftarrow PC + 1)$					
HLT	rB_0:	$S \leftarrow 0$					
Input-output:							
	$D_7IT_3 = p$	(common to all input-output instructions)					
	$IR(i) = B_i$	(i = 6, 7, 8, 9, 10, 11)					
	p:	$SC \leftarrow 0$					
INP	pB_{11}:	$AC(0\text{-}7) \leftarrow INPR, FGI \leftarrow 0$					
OUT	pB_{10}:	$OUTR \leftarrow AC(0\text{-}7), FGO \leftarrow 0$					
SKI	pB_9FGI:	$If (FGI = 1) then (PC \leftarrow PC + 1)$					
SKO	pB_8FGO:	$If (FGO = 1) then (PC \leftarrow PC + 1)$					
ION	pB_7:	$IEN \leftarrow 1$					
IOF	pB_6:	$IEN \leftarrow 0$					