Final Winter 2005

Name: Solution Student #: Section:

Question	Max Marks	Score
1	10	
2	20	
3	25	
4	25	
5	20	
Total	100	

CARLETON UNIVERSITY

FINAL
EXAMINATION
April 29, 2005

Duration: 3 hours

Department name and course number: Electronics ELEC-2507 (A,B,C)

Course Instructor(s): R. Mason, A. Steele Number of students: 220

AUTHORIZED MEMORANDA:

NON-PROGRAMMABLE CALCULATOR

Students MUST count the number of pages in this examination paper before beginning to write, and report any discrepancies immediately to a proctor. **This question paper has 17 pages.**

This examination question paper MAY NOT be taken from the examination room.

This exam consists of 5 questions, which should be answered on this exam paper in the space provided. Attempt all questions. Marks allocated to each question are indicated (total marks = 100).

Note: The solution must be clearly indicated. Multiple solutions or solutions that are not clearly identified, will be marked incorrect. Using approximate relations (unless they are given below or specified in a question) is not accepted. Clearly state all assumptions made. **Clearly mark the units for all final answers. Clearly indicate axis/units for any graphs. SHOW YOUR WORK!**

Diode:

Forward current: $I_D \approx I_S\left(e^{V_D/nV_T}\right)$

Small signal resistance: $r_d = \frac{nV_T}{I_D}$

$V_T = \frac{kT}{q} = 25mV$ at room temperature

Bipolar Transistor:

Active mode operation: $V_{BE} = 0.7V$

Saturation mode operation: $V_{CEsat} = 0.2V$

$i_C = \beta i_B \quad i_C = \alpha i_E \quad i_E = i_B + i_C$

$g_m = \frac{I_C}{V_T} \qquad r_\pi = \frac{\beta}{g_m} \qquad r_o = \frac{V_A}{I_C}$

$r_e = \frac{\alpha}{g_m} = \frac{r_\pi}{\beta+1} \qquad \alpha = \frac{\beta}{\beta+1}$

Operational Amplifier:

$V_o = A(V_+ - V_-);\ R_i = \infty;\ R_o = 0$

MOSFET:

$I_{DS} = k'\frac{W}{L}\left[(V_{GS} - V_t)V_{DS} - \frac{V_{DS}^2}{2}\right];$

$I_{DS,sat} = k'\frac{W}{L}\frac{(V_{GS} - V_t)^2}{2}(1 + \lambda V_{DS});$

$k' = \mu C_{ox}; \quad K = k'\frac{W}{L}$

$V_{DS,sat} = V_{GS} - V_t \qquad g_{mb} = \chi g_m$

$g_m = k'\frac{W}{L}(V_{GS} - V_t) = \sqrt{2k'\frac{W}{L}I_{DS}}$

$r_{DS,triode} = \left[k'\frac{W}{L}(V_{GS} - V_t)\right]^{-1}; \quad r_o = \frac{V_A}{I_D}$

Q1: Answer the following by filling in the corresponding circles with your selection *a, b, c or d*

(10 marks).

i) Assuming all diodes have a forward bias turn on voltage of 0.7V which statement best describes how the circuit in Fig. 1.1 operates?

a) LED1 is illuminated when V_i is -5V
b) LED2 is illuminated when V_i is -5V
c) Both LED1 and LED2 are illuminated when V_i is 5V
(d) ✓d) LED2 is illuminated when V_i is 5V

*1) Only for $V_i > 0.7$ (positive values of the input voltage) diodes in either branches can be in Forward bias.
(So, (a) & (b) can not be true)

*2) As soon as LED2 turns ON it keeps $V_{AB} = 0.7V$. This prevents LED1 (in series with D1) to be illuminated.

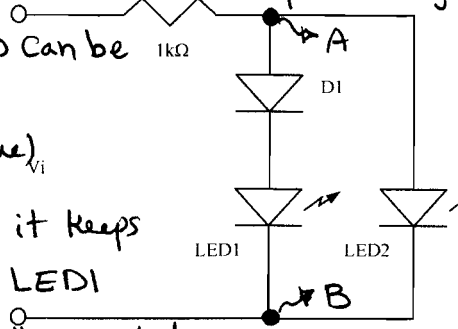


Fig 1.1

⚠ Technical explanation:
For the sake of simplicity, in this answer LEDs are treated as the same way with non-ideal diodes as D_1.
However, one should note that, this is not a practical assumption. Then, any conclusion based on this assumption may not be always verified in all practical examples.

ii) Which one of the following statements best describes a forward biased silicon diode?

NOTE: $i_D = I_S(e^{v_D/nV_T} - 1) \approx I_S e^{v_D/nV_T}$

(a) a) The current through the diode is exponentially related to the diode voltage
b) The voltage across the diode is 0 volts
c) The current through the diode is of the form kV_D^2 where k is a constant and V_D is the diode voltage
d) The current through the diode is 0 amps

iii) A npn BJT has I_B=1uA and β=100. Which of the following statements is true?

$I_C = \beta I_B = 100 \times 1\mu A = 100\mu A$
A typical value for V_{BE} in "active mode operation" is $V_{BE} = 0.7V$ (which is close to 1 (ONE), here)

(d) a) I_C=100uA, V_{CE}=0.01V, the devices is operating in active mode
b) I_C=10uA, V_{CE}=1V, the devices is operating in saturation mode
c) I_C=1000uA, V_{CE}=0.01V, the devices is operating in saturation mode
d) I_C=100uA, V_{CE}=1V, the devices is operating in active mode

iv) Which of the following best describes how we can increase the small signal voltage gain of a standard BJT common emitter amplifier?

Considering: $|A_v| \approx g_m R_c$
R_c increases → $|A_v|$ increases (Provide I_c is kept constant). ⇒ For C ✓

(a & c) ✓a) increase the power supply voltage
b) decrease the transistor output resistance
✓c) increase the collector resistance
d) decrease the transistor β

For a:
Also, if the power supply voltage increases it causes, I_c may increase.
Since $g_m = \frac{I_c}{V_T}$; any increase in I_c would results g_m to increase & consequently it increases the A_v.

$V_{power\ supply} \uparrow \longrightarrow I_c \uparrow \longrightarrow g_m \uparrow \longrightarrow |A_v| \uparrow$

v) What is the value of V_C for the circuit in Fig. 1.2

Typical value in active mode operation

KVL at B-E Loop:

$-2 + 10K I_B + V_{BE} + 1.5 = 0$, where $V_{BE} = 0.7$

$I_B = \frac{2 - 1.5 - 0.7}{10K} = \frac{-0.2}{10K} < 0$ *

(b) a) 8.7V
b) 10V
c) 0V
d) 1.7V

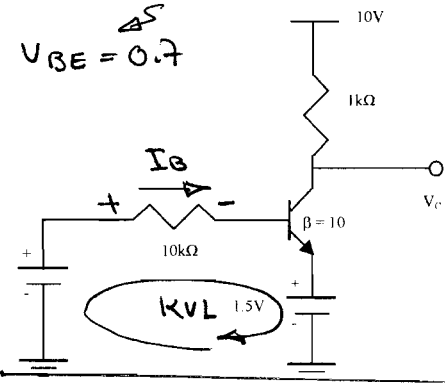


Fig. 1.2

* Negative value for I_B from above calculation means that BJT in this circuit can NOT be ON. Tr: OFF ⇒ $I_C = 0$ & $V_C = 10V - 1K\Omega \times I_C$

$= 10V - 1K\Omega \times 0$

$= 10V$

Handwaving; Since a 2 Volts Source is NOT enough to provide $V_{BE} = 0.7$ Volts, when V_E is directly connected to a 1.5 Volts Battery. ∴ So, Tr: off ⇒ $V_C = 10V$

vi) Which of the following is NOT a characteristic of an ideal operational amplifier?

(b) a) infinite input impedance
b) zero common-mode rejection
c) zero output resistance
d) infinite open-loop gain

vii) Which is the best description of the circuit in figure 1.3?

(d) a) unity gain amplifier
b) a buffer
c) an integrator
d) a differentiator

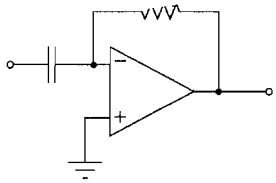


Fig 1.3

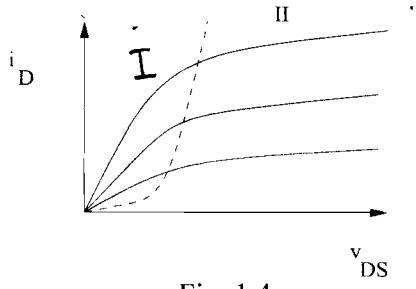


Fig. 1.4

viii) Figure 1.4 shows a sketch of the $i_D - v_{DS}$ characteristic curves for a MOSFET. What are regions I and II known as?

(C) a) I-triode II-active
b) I-cut-off II-saturation
c) I-triode II-saturation
d) I-cut-off II-triode

Practice Question:

Answer the similar question for a BJT.

ix) Examine the circuit in Fig. 1.5. Which statement below is correct?

a) $V_{DS} = V_{DD} + R_D I_D$
b) $V_{DS} = V_{GS}$
c) $V_{DS} = V_{GS} + R_G I_D$
d) $V_{DS} = V_{DD}$

(b)

Hint: $I_G = 0$ (always)

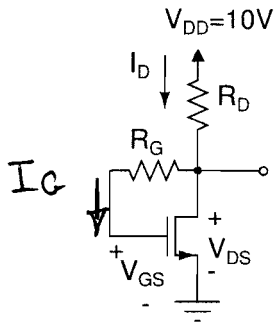


Fig. 1.5

x) A transistor amplifier has the following measure characteristics for two different load resistances.

Load resistance	Input voltage / mV	Output voltage /mV
Without R_L	8	80
With $R_L = 5$ kΩ	7	60

In this question it is assumed that the above measurments have been performed using 2 different values for the input source. (8mV when No load & 7mV when there was a load)

Calculate the open circuit voltage gain, A_{VO}, the voltage gain with the 5 kΩ load resistor, A_V and the output resistance, R_o. Which of the following best matches the calculated parameters?

a) $A_{VO} = 10$, $A_V = 11.7$ and $R_o = 5$ kΩ
b) $A_{VO} = 8.6$, $A_V = 10$ and $R_o = 1.3$ kΩ
c) $A_{VO} = 10$, $A_V = 7.5$ and $R_o = 1.7$ kΩ
d) $A_{VO} = 10$, $A_V = 8.6$ and $R_o = 0.8$ kΩ

(d)

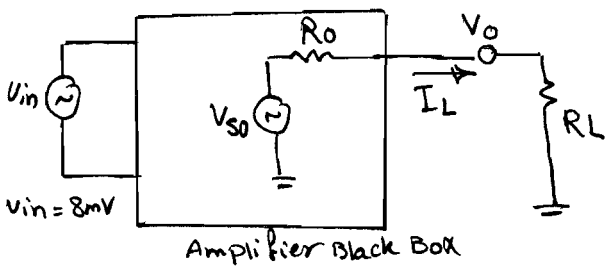
① Open Circuit voltage gain (No Load)

$$|A_{V0}| = \frac{|V_{out}|}{|V_{in}|} = \frac{80mV}{8mV} = 10\ V/V$$

2) The voltage gain when there is a load as $R_L = 5k\Omega$ connected to the output.

$$|AV| = \frac{|V_{out}|}{|V_{in}|} = \frac{60mV}{7mV} = 8.57\ V/V$$

3) To decide the output resistance, R_o, let the Thevinen' equivalent circuit of the amplifier output look be considered as shown below



(a) $V_{in} = 8mV \Rightarrow V_{o(NoLoad)} = 80mV \Rightarrow$ { since $I_L = 0$ } $V_{SO} = 80mV$

(b) with Load & $V_{in} = 8mV \Rightarrow V_{o(Load)} = 8.57 \times 8m = 68.56$ mV

$$V_{o(Load)} = 68.56m \Rightarrow I_L = \frac{68.56}{5K} = 13.7\mu A$$

(c) $V_{Ro} = V_{SO} - V_{o(Load)} = 80mV - 68.56 = 11.44mV$

$$R_o = \frac{V_{Ro}}{I_L} = \frac{11.44mV}{13.7\mu A} = 835\Omega \approx 0.8k\Omega$$

Q2: Diodes

a) The circuit has been designed in Fig. 2.1, with diodes having forward voltages of 0.7V.

(i) If V_A = -3V V_B = 0.7V, V_C = 5V and V_D = 3V, what will be the output at Vx and the current I? If voltage V_A, V_B, V_C and V_D could only be 0V or 5V this circuit could be used as a logic gate. What type of gate would it be? **(4 Marks)**

⇒ Diode "C" is ON &

$V_X = 5 - 0.7V = 4.3V$

$V_D = 0.7V$

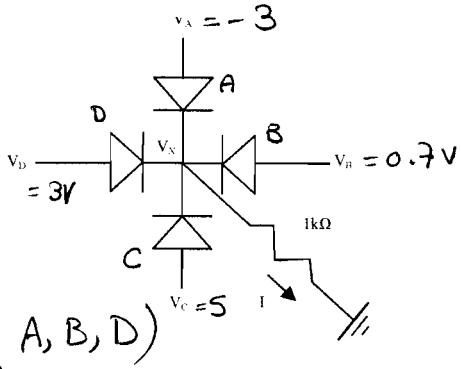


Fig. 2.1

⇒ having V_X at 4.3V, applied to the cathodes of all other Three diodes (A, B, D) keeps them in Backward bias & ensures them OFF.

So, $I = \frac{V_X}{R} = \frac{4.3V}{1K\Omega} = 4.3mA$

V_X = 4.3V

I = 4.3mA

Logic Gate Type = OR Gate

b) A zener diode circuit has been designed using two identical zener diodes as shown in Fig. 2.2.

The zener data for each diode is V_z = 4 V at I_z = 2 mA, r_Z = 20Ω and I_{zk} = 0.5 mA.

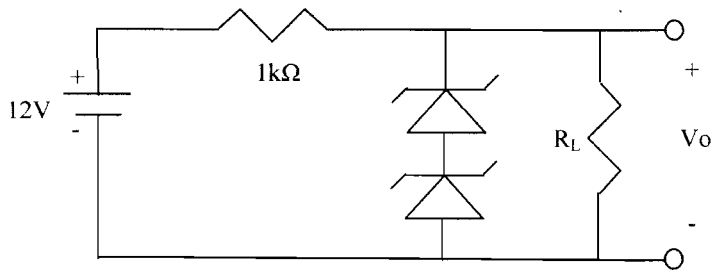


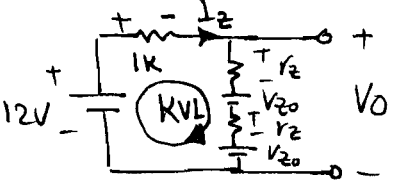
Fig. 2.2

Answer the following questions:

i) Find the DC value of V_O **with no load resistor** (R_L). **(4 Marks)**

* Assume the diodes are ON.

$V_z = V_{z0} + r_z I_z \rightsquigarrow 4V = V_{z0} + 20 \times 2m \Rightarrow V_{z0} = 4 - 0.04 = 3.96V$



KVL: $-12 + 1K I_z + 2r_z I_z + 2V_{z0} = 0$

$I_z = \frac{12 - 2V_{z0}}{1K + 2r_z} = \frac{12 - 2(3.96)}{1K + 2(20)} = 3.92mA > I_{zK}$ * ✓

$V_O = 12 - 1K(3.92mA) = 8.08V$ $V_O =$ 8.08V

* Note, having $I_z > I_{zK}$ the assumption of diodes are ON is verified!

ii) Find the change in V_O if the 12V power supply were to vary by ±1V. **(2 Marks)**

For above circuit the "Line Regulation" eqn can be adapted as:

$\frac{\Delta V_O}{\Delta V_S} = \frac{2r_z}{R + 2r_z} \Rightarrow \Delta V_O = \frac{2(20)}{1K + 2(20)} \Delta V_S$

$\Delta V_O = \frac{40}{1040} \Delta V_S = 0.0385 \Delta V_S$ $\Delta V_O =$ ±0.0385 ΔV_S

iii) For the nominal 12V supply, what is V_O if a 10kΩ load resistor, R_L, is added? **(3 Marks)**

Assuming both D_{z1} & D_{z2} are ON. As an appropriately approximated solution, assume that connecting R_L does NOT effect V_O the value calculated in (i) above.

$\Delta I_z = I_L \approx \frac{V_O(\text{load})}{R_L} = \frac{V_O(\text{No load})}{10K} = \frac{8.08V}{10K} \approx 0.808mA$

$I_z(\text{with load}) \approx I_{z(\text{No Load})} - \Delta I_z = 3.92mA - 0.808m = 3.112mA > I_{zK}$ ✓ assumption of D_z are ON is verified!

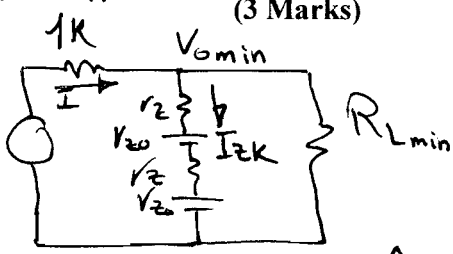
$V_O(\text{w. Load}) = 2V_{z0} + 2r_z I_{z(\text{w.load})} = 2 \times 3.96 + 2(20)(3.112mA)$ $V_O =$ 8.044V
$= 8.044V$

The most accurate solution using mesh analysis results in: $I_L = 0.8046$ mA (0.8046mA) which is quite close to our answer here.

iv) For the nominal 12V supply, compute the minimum value of R_L so that the output is maintained at a relatively constant output. **(3 Marks)**

For the minimum value of R_L (worst case) the zeners are assumed to be at the edge of the break down region which is

$I_z = I_{zK} = 0.5mA$



$V_{omin} = 2V_{z0} + 2r_z I_{zK} = 2 \times 3.96 + 40 \times 0.5mA = 7.922V$

$I_{1K} = \frac{12 - 7.922}{1K} = 4.078mA$ $I_{R_{Lmin}} = I_{1K} - I_{zK} = 4.078mA - 0.5mA = 3.578mA$

$R_{Lmin} = \frac{V_{omin}}{I_{R_{Lmin}}} = \frac{7.922}{3.578m} = 2.214K\Omega$ $R_{Lmin} =$ 2214Ω //

c) A square wave input as shown below is applied to V_i of the ideal diode circuit in Fig. 2.3.

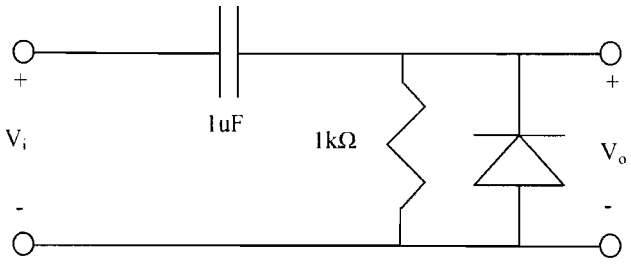
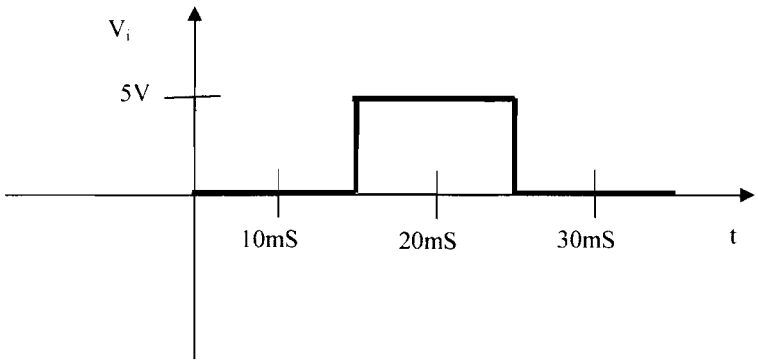
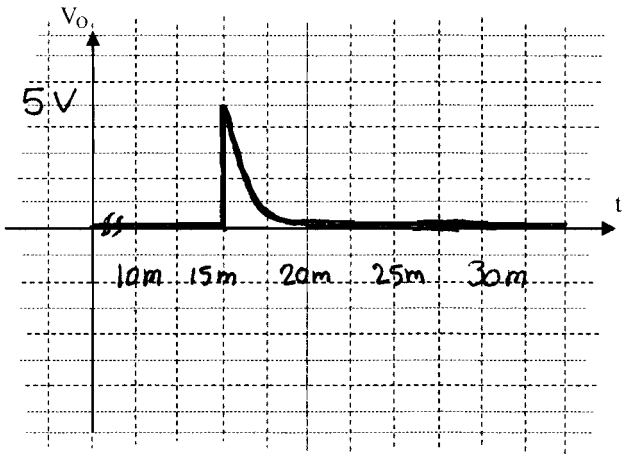


Fig. 2.3



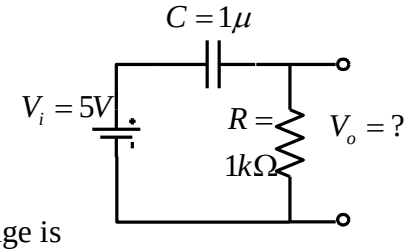
Sketch the resulting waveform at Vo assuming the initial value of Vo is 0V. Make sure to include scales on the voltage and time axis **(4 Marks)**



(Page 7 of 17) Q2_part C answer:

- The time constant τ for this RC circuit is $\tau = RC = 1k \times 1\mu = 1\text{msec}$
- The pulse width of the input signal is $T_W = 10\text{msec}$

1) for $t < 15\text{msec}$: since the input source is zero $(V_i = 0)$; the voltage at output is zero $(V_o = 0)$;
2) At $t = 15\text{msec}$: the capacitor will see an instant change in input voltage (from 0-to-5V) and (instantly) acts as a short circuit. This means that, V_o will follow the input $(Vo = 5V)$
3) $15\text{msec} < t \le 25\text{msec}$: at 15msec the capacitor starts charging, and continues charging as time passes. The equivalent circuit is shown to the right.



$15m < t \le 25m$: $V_O = V_m e^{\frac{-t_a}{\tau}} = 5e^{\frac{-t_a}{1m\text{sec}}}$

Say:

- at $t = 16\text{msec}$, capacitor charged for 1msec
  $t_a = 1m\text{sec}\ (\rightarrow 16m\text{sec} - 15m\text{sec})$, then the output voltage is
  $V_o = 5e^{-\frac{1m\text{sec}}{1m\text{sec}}} = 5 \times 0.37 = 1.84V$

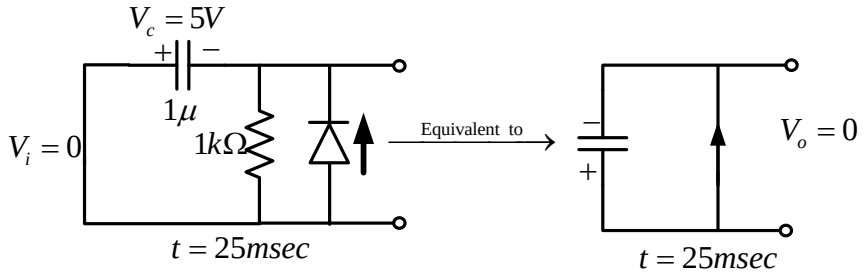
Similarly, say:

- at $t = 17m\text{sec} \rightarrow t_a = 17m\text{sec} - 15m\text{sec} = 2m\text{sec} \rightarrow V_o = 5e^{-\frac{2m\text{sec}}{1m\text{sec}}} \approx 1V$
- at $t = 18m\text{sec} \rightarrow t_a = 18m\text{sec} - 15m\text{sec} = 3m\text{sec} \rightarrow V_o = 5e^{-\frac{3m\text{sec}}{1m\text{sec}}} \approx 0.25V$
- at $t = 19m\text{sec} \rightarrow t_a = 19m\text{sec} - 15m\text{sec} = 4m\text{sec} \rightarrow V_o = 5e^{-\frac{4m\text{sec}}{1m\text{sec}}} \approx 0.09V$
- at $t = 20m\text{sec} \rightarrow t_a = 20m\text{sec} - 15m\text{sec} = 5m\text{sec} \rightarrow V_o = 5e^{-\frac{5m\text{sec}}{1m\text{sec}}} \approx 0.034V \approx 0$

This means, the capacitor has been fully charged to 5V and will stay charged until 25msec.

Since in this circuit $\tau << T_W$; it does not behave as a regular diode clamper circuit.

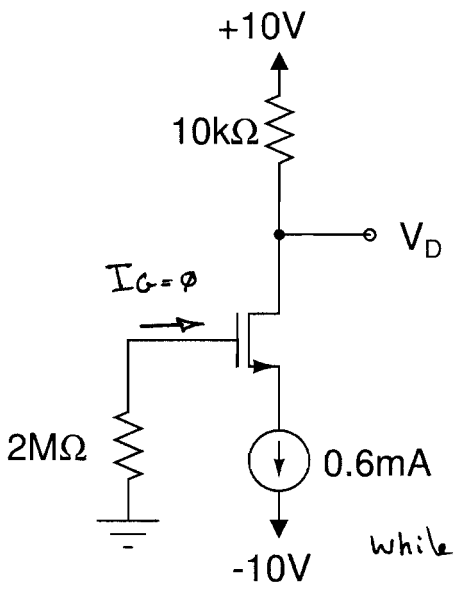
4) at $t = 25\text{msec}$: The input instantly decreases by 5V and falls to 0V, as seen below the charge across the capacitor appears right across the diode and this causes the diode to conduct heavily and to quickly discharge the capacitor.



5) at $t > 25\text{msec}$: The input source $V_i = 0$ and capacitor has been already discharged and $V_c = 0$, therefore the voltage at the output will be (and stay at) zero, $V_o = 0$.

Q3: MOSFET

The MOSFET circuit shown in Fig, 3.1 is biased by a constant current source.



$I_G = 0 \Rightarrow V_G = 0V$

$I_D = I_S = 0.6mA$

$V_D = 10V - 10K \times 0.6mA = 10V - 6V = 4V$

Assume MOSFET operates in saturation mode.

Accordingly it is expected that,

$V_{GS} - V_t \leq V_{DS}$ or equivalently

$V_G - V_t \leq V_D \quad (*)$

while we have $0 - 1.5V < 4V \Rightarrow$ So, the above assumption is true!

Fig. 3.1

a) Given $V_t = 1.5$ V, $k'_n = 120\ \mu A/V^2$ and W/L = 10

i. Find the following voltages, V_{GS}, V_G, V_S and V_D. **(5 Marks)**

Sat. $\Rightarrow I_D = \frac{1}{2} k'_n \frac{W}{L} (V_{GS} - V_t)^2 \rightsquigarrow 0.6mA = \frac{1}{2} \times 120\mu \times 10 (V_{GS} - V_t)^2$

$(V_{GS} - V_t)^2 = \frac{1.2m}{120\mu \times 10} = 1 \rightsquigarrow V_{GS} - 1.5V = \pm 1 \Rightarrow V_{GS} = \begin{cases} 0.5V \\ 2.5V \end{cases}$

Let us see which one of the calculated V_{GS} above can satisfy the starting assumption of saturation by holding eqn $(*)$ above.

1) $V_{GS} = 0.5 \rightsquigarrow V_G - V_t = 0.5 - 1.5 = -1 < 0$ this value can NOT be accepted because if so, $V_{GS} < V_t$ & this means Tr is OFF (& NOT sat.)

2) $V_{GS} = 2.5V \Rightarrow V_G - V_S = 2.5V \Rightarrow 0 - V_S = 2.5V \Rightarrow V_S = -2.5V$

EXTRA NOTE:

Again it is easily seen that, $V_{GS} - V_t = 2.5 - 1.5 = 1V < V_{DS} = 4V$ ✓

V_{GS} 2.5V V_G 0 V_S −2.5 V_D 4V

ii. Calculate g_m & r_0 given V_A = 80V. **(2 Marks)**

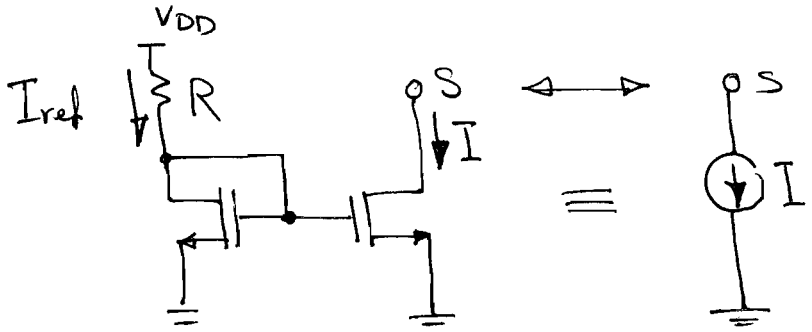
$$g_m = \sqrt{2k'\frac{W}{L} I_{DS}} = (2 \times 120\mu \times 10 \times 0.6m)^{1/2}$$

$$= 1.2 \times 10^{-3} = 1.2\ m\ I/V$$

$$r_o = \frac{|V_A|}{I_D} = \frac{80}{0.6\ m} = 133.33\ K\Omega$$

g_m 1.2 m I/V r_0 133.33 KΩ

iii. A MOSFET circuit that could be used as the constant source in Fig 3.1 is called the current mirror. Sketch the basic MOSFET current mirror circuit. **(3 Marks)**



b) The circuit is modified so that it can be used as a small-signal amplifier. The new circuit, with the signal source, is shown in Fig. 3.2

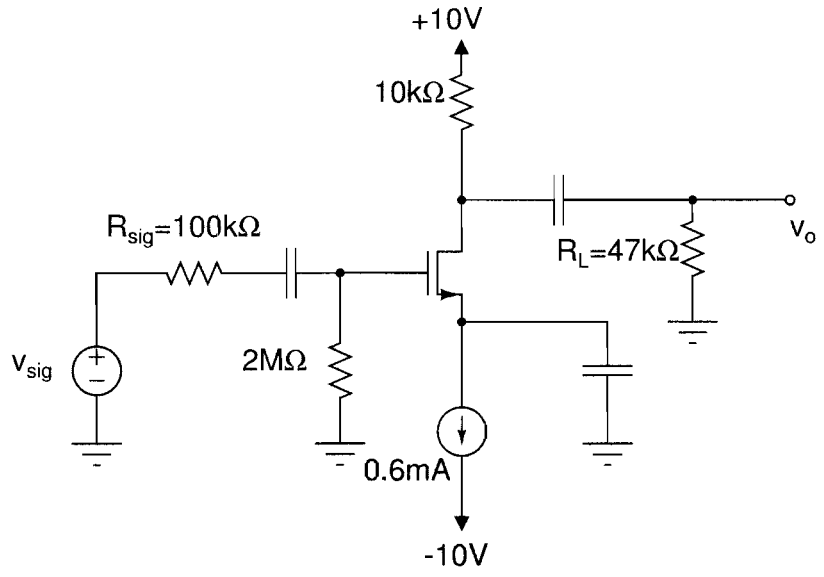
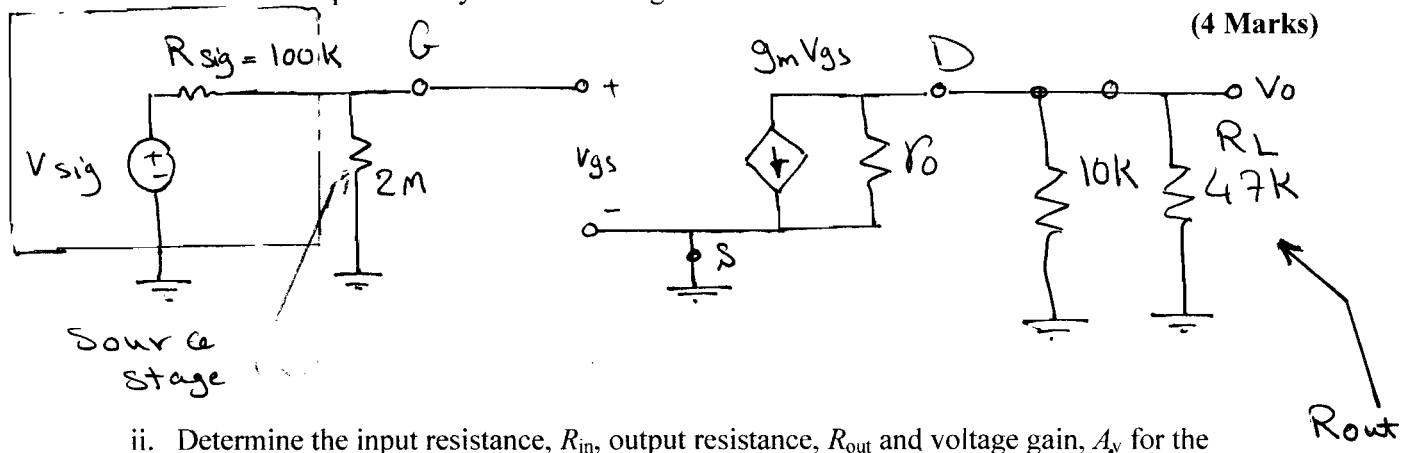


Fig. 3.2 (Assume all capacitors have an infinite value).

i. Sketch the equivalent hybrid-π small signal circuit model for this circuit. **(4 Marks)**



ii. Determine the input resistance, R_{in}, output resistance, R_{out} and voltage gain, A_v for the amplifier (take into account r_o & R_L). **(3 Marks)**

$R_{in} = 2M\Omega$, According to the Fig. $R_{out} = r_o \| 10K \| 47K$ (*)

$= 133.33K \| 10K \| 47K = 7.764K$

Overal voltage gain $A_V = \frac{V_o}{V_{sig}} = \underbrace{\frac{V_{gs}}{V_{sig}}}_{A_{V1}} \times \underbrace{\frac{V_o}{V_{gs}}}_{A_{V2}}$

$= \left(\frac{2M}{2M+100K}\right) \times \left(-g_m \times r_o \| R_D \| R_L\right)$

$= \frac{2}{2.1} \times -1.2m \times 7.764K = 0.95 \times (-9.32)$

$= -8.87\ V/V$

R_{in} 2MΩ R_{out} 7.764KΩ A_v −8.87 V/V

(*) NOTE: ONE may want to consider & calculate Rout before R_L, which is also an acceptable case then, $R_{out}|_{\text{before } R_L} = r_o \| 10K \approx 9.3K\Omega$

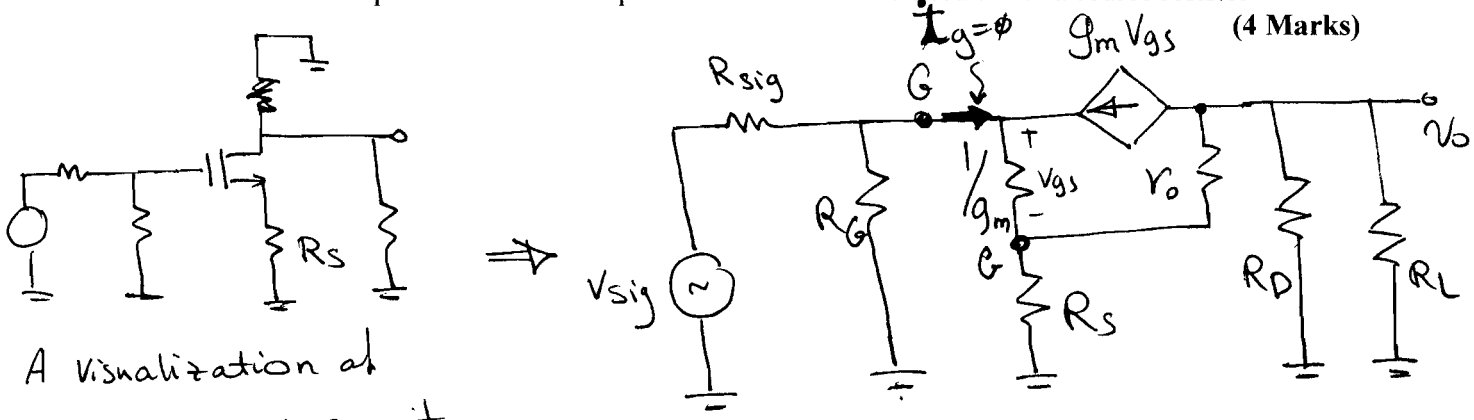
iii. If v_{sig} is a 0.2 V peak-to-peak sinusoid and assuming small-signal operation, what output signal v_o results if R_{sig} and R_L are 100kΩ and 47kΩ, respectively? **(2 Marks)**

$$\frac{v_o}{v_i} = A_v \rightsquigarrow v_o = A_v v_i = -8.87 \times 0.2V$$
$$= -1.774V$$

v_o 1.774 @ 180° phase shift

c) A resistor is now place into the source branch of the circuit (after the MOSFET source terminal and prior to the capacitor and current source).

i. Sketch the equivalent T-model equivalent circuit for this circuit with a source resistor **(4 Marks)**



A visualization of ac equivalent circuit including new Rs

Small signal equivalent of amplifier circuit using T-model for MOSFET

ii. State what will happen to the output v_o now that the source resistor is inserted. (Note, you do not need to perform analysis, just state what will happen). **(2 Marks)**

EXTra Explanation:

Let consider the overal voltage gain eqn s before & after adding Rs in below. (Neglecting r_o)

without Rs: $G_V = \frac{-R_G}{R_G + R_{sig}} \times g_m (R_D \| R_L)$

with Rs: $G_V = \frac{-R_S}{R_G + R_{Sig}} \times \frac{g_m (R_D \| R_L)}{1 + g_m R_S}$

NOTE: Adding Rs to a common source stage provides some improvments in performance BUT at the expense of reduced gain

ANS.: The overal voltage gain G_V of the amplifier is reduced. With reduced gain, V_o would have smaller magnitude for the same V_{sig} at input.

Q4: BJT

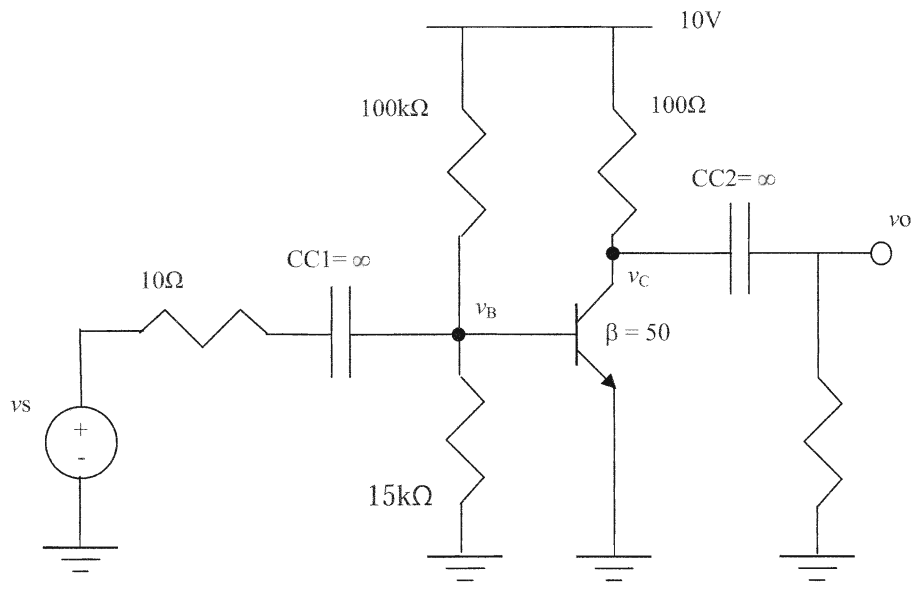
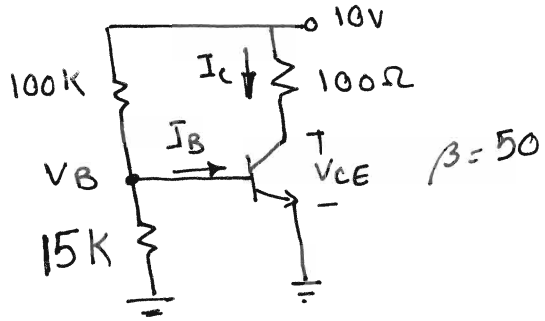


Fig. 4.1

a) For the BJT amplifier circuit shown in Fig. 4.1:

i) Draw the DC equivalent circuit that can be used for calculating DC voltages and currents **(3 Marks)**

For dc equivalent circuit, all cap should be treated as open circuit.



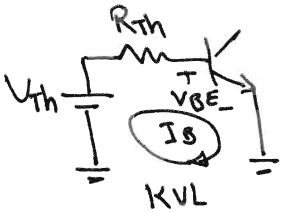
ii) Assuming room temperature, determine values for V_B, V_C, I_B, and I_C (where V_B etc. have their usual meaning): **(7 Marks)**

↳ $V_T = 25mV$ & $V_{BE} = 0.7$ Typical Values for active mode

So: $V_B = V_{BE} = 0.7V$

as Emitter is directly connected to the ground.

Considering Thevenin equivalent circuit for the 2-Resistor biasing Network as:



$R_{Th} = 100K \| 15K \approx 13K\Omega$

$V_{Th} = \frac{15K}{115K} \times 10V \approx 1.3V$

KVL at BE side:

$-V_{Th} + R_{Th} I_B + V_{BE} = 0$

$I_B = \frac{V_{Th} - V_{BE}}{R_{Th}} = \frac{1.3-0.7}{13K} \approx 46\mu A$

$I_C = \beta I_B = 50 \times 46\mu A = 2.3mA$

$V_C = 10 - R_C I_C = 10 - 2.3mA \times 100 = 9.77V$

$V_C = 9.77V$

$V_B = 0.7V$

$I_B = \approx 46\mu A$

$I_C = \approx 2.3mA$

4. b)

i) The BJT in figure 4.1 had an early voltage of 500V. Compute parameters r_π, g_m, and r_o,

(3 Marks)

$g_m = \frac{I_C}{V_T} = \frac{2.3mA}{25mV} = 0.092\ (A/V)$

$|V_A| = 500V \rightsquigarrow r_o = \frac{|V_A|}{I_C} = \frac{500V}{2.3mA} = 217,391 \approx 217K\Omega$

$r_\pi = \frac{V_T}{I_B} = \frac{25mV}{46\mu A} = 543.5\Omega$

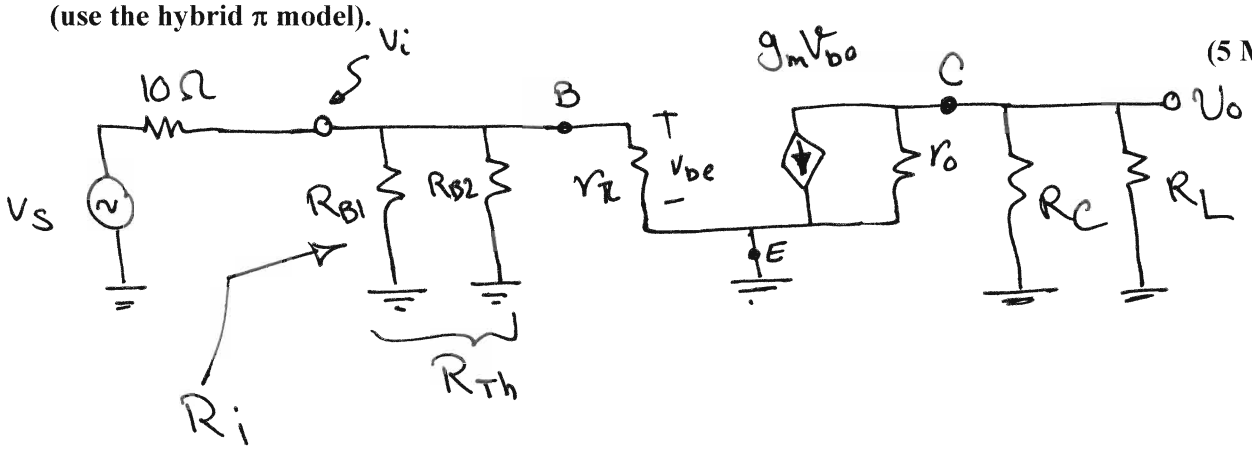
$g_m = 0.092\ (A/V)$

$r_o = 217K\Omega$

$r_\pi = 543.5\Omega$

ii) Draw the small signal A. C. equivalent circuit based on parameters calculated above in 4 b) **(use the hybrid π model).**

(5 Marks)



iii) Find the input resistance R_i

(2 Marks)

$R_i = R_{B1} \| R_{B2} \| r_\pi = R_{Th} \| r_\pi =$

$13K\Omega \| 543.5\Omega = 521.7\Omega$

$R_i = 521.7\Omega$

iv) Find the intermediate voltage gain, $A_{v1} = v_i/v_s$.

(1 Mark)

$$A_{vi} = \frac{V_i}{V_s} = \frac{R_i}{R_s + R_i} = \frac{521.7}{10\Omega + 521.7} = 0.98$$

$A_{v1} = 0.98\ V/V$

(v) Find the intermediate voltage gain $A_{v2} = v_o/v_i$.

(3 Marks)

$$A_{v2} = \frac{V_o}{V_i} = \frac{V_o}{V_{be}} = -g_m(r_o \,||\, \underbrace{R_c \,||\, R_L}_{R'_L})$$

$R'_L = R_c \,||\, R_L \approx R_c = 100\Omega$

also $r_o \,||\, R_c \approx R_c$

$A_{v2} = -0.092 \times 100 = -9.2\ (V/V)$

Since R_L is NOT given, Considering that, R_L is generally in the range of few KΩ, so $R_L \gg R_c$ & $R'_L = R_c \,||\, R_L \approx R_c$

$A_{v2} = -9.2\ (V/V)$

(vi) Find the overall voltage gain, $A_v = v_o/v_s$.

(1 Mark)

$$A_V = \frac{V_o}{V_s} = \frac{V_o}{V_i} \times \frac{V_i}{V_s} = A_{V2} \times A_{Vi}$$

$A_V = -9.2 \times 0.98 = -9$

$A_v = \approx -9$

5. Operational Amplifier

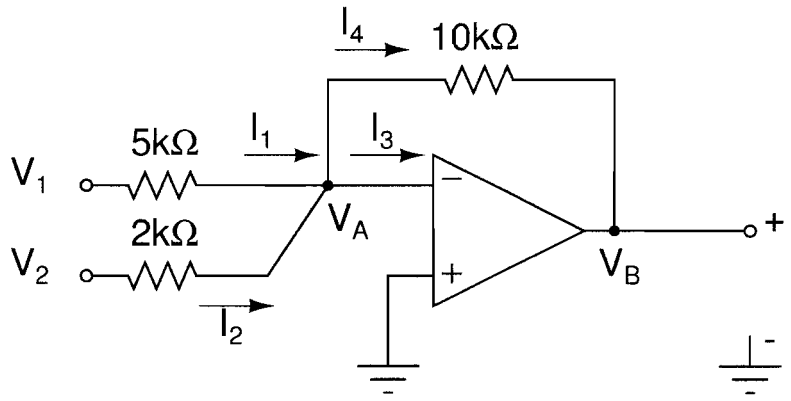


Fig. 5.1

a) Assuming ideal operational amplifiers (op-amps.), analyze the circuit in Fig. 5.1 and find expressions for the various branch currents and nodal voltages (as marked on the figure). Note: V_1 and V_2 are the inputs to the circuit. **(6 Marks)**

1) $V_A = V^- = V^+ = 0 \Rightarrow V_A = 0$ Virtual ground

2) $I_3 = \emptyset$

3) $I_1 = \frac{V_1 - V^-}{5K} = \frac{V_1}{5K}$ 4) $I_2 = \frac{V_2 - V^-}{2K} = \frac{V_2}{2K}$

5) $I_4 = \frac{V^- - V_B}{10K} = -\frac{V_B}{10K}$

KCL @ A: $I_1 + I_2 - I_3 - I_4 = 0 \rightsquigarrow \frac{V_1}{5K} + \frac{V_2}{2K} - 0 - \left(-\frac{V_B}{10K}\right) = 0$

$V_B = -\left(\frac{10K}{5K}V_1 + \frac{10K}{2K}V_2\right) = -2V_1 - 5V_2$

$I_1 = \frac{V_1}{5K}$ $I_2 = \frac{V_2}{2K}$ $I_3 = \emptyset$ $I_4 = \frac{-V_B}{10K}$ $V_A = \emptyset$ $V_B = -2V_1 - 5V_2$

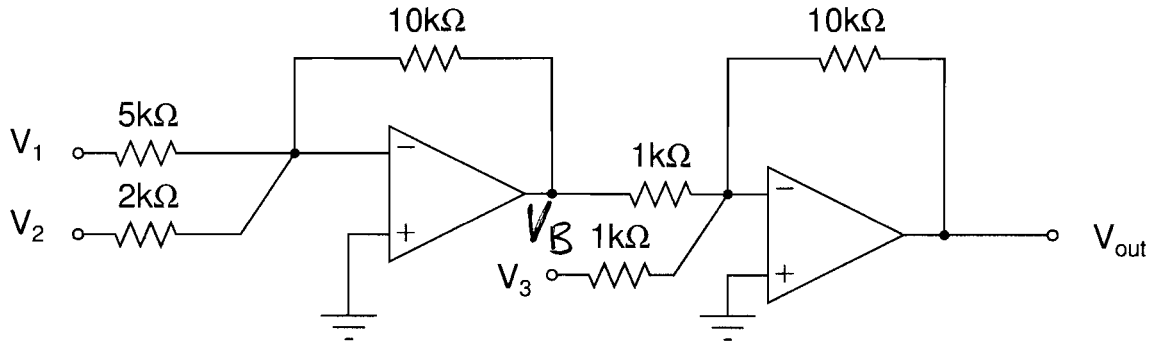


Fig. 5.2

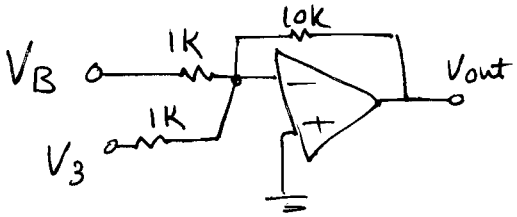
b) The circuit in a) is now used to make a larger circuit, see Fig. 5.2. The intention is for this circuit to have the output response:

$$V_{out} = 2V_1 + 5V_2 + 10V_3 \qquad (5.1)$$

Measurements show that this circuit does not give the desired response, stated in (5.1)

i. Analyze the circuit and state the correct response of the proposed circuit. **(3 Marks)**

LET Analayze the output (last) stage first,



$$V_{out} = -\left(\frac{10K}{1K} V_B + \frac{10K}{1K} V_3\right) = -10V_B - 10V_3$$

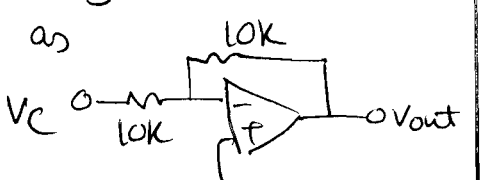
Knowing that, $V_B = -2V_1 - 5V_2$

$$V_{out} = -10(-2V_1 - 5V_2) - 10V_3$$

$$= 20V_1 + 50V_2 - 10V_3$$

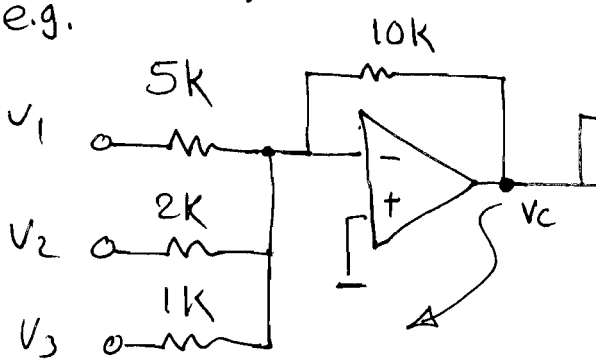
ii. Provide a circuit design that will give the response of (5.1) using only the components shown in Fig. 5.2, plus an extra 10 kΩ resistor. Note: you do not need to use all the components. **(4 Marks)**

* NOTE: The unity Gain inverting Stage can be also design as



Anyhow, both solutions are technically correct also there are other possible solutions too.

e.g.



Unity gain inverting buffer

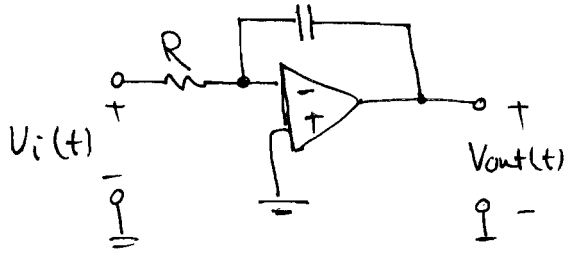
$V_{out} = -V_C$ (1)

$V_C = -2V_1 - 5V_2 - 10V_3$ (2)

(1) & (2) $\Rightarrow$ $V_{out} = 2V_1 + 5V_2 + 10V_3$

c) An op-amp. based inverting Miller integrator is measured at 1 kHz and found to have a voltage of -50V/V.

i. Sketch the basic circuit for an op-amp. inverting Miller integrator. **(2 Marks)**



$$\frac{V_{out}}{V_i} = -\frac{1}{sRC}, \quad \text{where } s = j\omega = j2\pi f$$

ii. At what frequency is the gain reduced to -1V/V? **(3 Marks)**

@ $f = 1\,kHz \Rightarrow \frac{V_o}{V_i} = -50 \Rightarrow -50 = -\left|\frac{1}{j\omega RC}\right|_{\omega = 2\pi \times 1K}$

$$50 = \frac{1}{2\pi \times 1K\,(RC)} \Rightarrow RC = \frac{1}{2\pi \times 1K \times 50} = \frac{10}{\pi}\,\mu\,sec$$

Now: @ $f_2 = ? \Rightarrow \frac{V_o}{V_i} = -1 \Rightarrow -1 = -\left|\frac{1}{j2\pi f_2 RC}\right| \Rightarrow 2\pi f_2 RC = 1$

$$f_2 = \frac{1}{2\pi RC} = \frac{1}{2\pi \times \frac{10}{\pi}\mu} = 50\,kHz$$

iii. Sketch the response of the magnitude of the gain (in dB) with respect to angular frequency (radians per second). **(2 Marks)**

dB: $20\log\left|\frac{V_o}{V_i}\right| = 20\log\left|\frac{-1}{2\pi jf} \times \frac{1}{RC}\right| = 20\log\left|\frac{\pi \times 10^5}{2\pi f}\right|$

$$\Rightarrow 20\log\left|\frac{V_o}{V_i}\right| = 20\log\left|\frac{50 \times 10^3}{f}\right|$$

freq.

Checking for few points

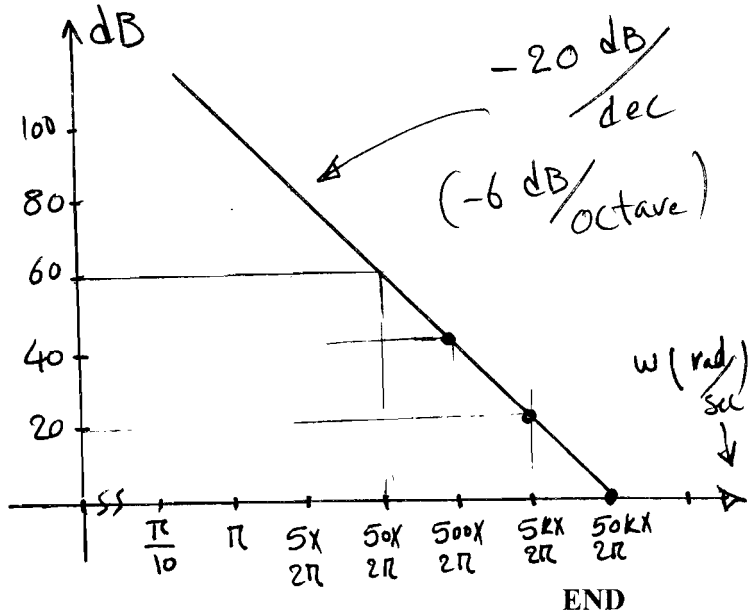
1) $f = 50K \Rightarrow 20\log\left|\frac{50k}{50k}\right| = 20\log 1 = 0\,dB$

2) $f = 5K \Rightarrow 20\log\left|\frac{50 \times 10^3}{5 \times 10^3}\right| = 20\,dB$

3) $f = 0.5K \Rightarrow 20\log\left|\frac{50 \times 10^3}{0.5 \times 10^3}\right| = 40\,dB$

.....

$f = DC$ Gain = infinity



END