Université d'Ottawa
Faculté de génie

École d'ingénierie et de
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University of Ottawa
Faculty of Engineering

School of Information
Technology and Engineering

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COURSE: CEG2136/CEG2536
Computer Architecture I
Architecture des ordinateurs I

SEMESTER: Fall 2008

PROFESSORS:
Voicu Groza
Aziz Abdesselam

DATE: October 25, 2008

TIME: 13h00 – 14h30

MIDTERM EXAMINATION

NAME and STUDENT NUMBER:_____/_____

Instructions:

- Answer ALL questions on the questionnaire.
- This is a close-book examination**.**
- Use the provided space to answer the following questions. For your calculations you can use pages 6-8.
- Calculators are not allowed.
- Read all the questions before you start.

Q1. The range of signed integers N expressed in *2-s complement representation* that can be stored in a 10-bit register is: 1 point

(a) $-1024 \leq N \leq +1023$ (b) $-1023 \leq N \leq +1024$ (c) $-512 \leq N \leq +511$ (d) $-511 \leq N \leq +512$

(e) None of the above

Q2. Identify the decimal number which is represented next in floating point with the IEEE 754 standard: 11000001010001010110000000000000 1.5 points

(a) $(-133.375)_{10}$ (b) $(-69.375)_{10}$ (c) $(-138.750)_{10}$ (d) $(-34.6875)_{10}$ (e) $(-8.671875)_{10}$

Q3) Give the best binary approximation of $A = (26.6)_{10}$ and $B = -(23.4)_{10}$ employing *signed 2's-complement representation* with 2 bits for the fractional part. 1.5 points

A = B =

Q4) Two 6-bit registers contain two numbers X = 01010 and Y = 10101 (expressed in 2's complement representation). Using additions and 2's complementation only, calculate

- the sum (**S = X+Y**) and 1 point
- the difference (**D=X-Y**) 1.5 points

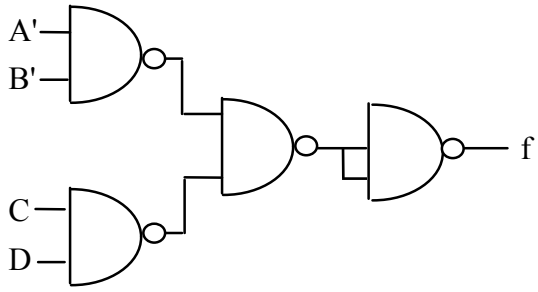
Convert in decimal and write each intermediate and final result, to check the correctness of your assertions.

S = X+Y 2's complement Base 10 **D=X-Y** 2's complement Base 10

CY:								CY:						
X +								X +						
Y								-Y						
S								D						

- Since both S and D have to be represented with 6 bits, indicate if overflow occurs; give the logic equation of a circuit which can detect such situations. 1 point

Q5. Which of the logic functions is implemented by the following circuit? 1.5 points



(a) f(A,B,C,D) = Σm(4,5,6,7,8,9,10)+X(12,13,14,15)

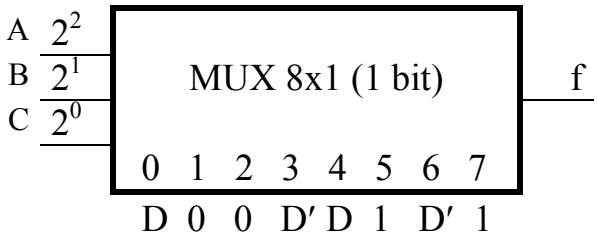
(b) f(A,B,C,D) = Σm(4,5,6,8,9,10,14)

(c) f(A,B,C,D) = Σm(0,1,2,3,6,7,14,15)

(d) f(A,B,C,D) = Σm(0,1,2,3,7,11,15)

(e) f(A,B,C,D) = Σm(4,5,6,8,9,10,12,13,14)+X(7,11)

Q6. Which of the following logic functions is implemented by the given circuit? 1.5 points



(a) f(A,B,C,D) = Σm(2,5,9,10,11,12,13,15)

(b) f(A,B,C,D) = Σm(0,7,8,10,11,13,14,15)

(c) f(A,B,C,D) = Σm(3,4,9,10,11,12,13,15)

(d) f(A,B,C,D) = Σm(3,5,6,7,8,12,13,15)

(e) f(A,B,C,D) = Σm(1,6,9,10,11,12,14,15)

Q7. What is the capacity of a ROM, capable to implement three functions de six variables? 1.5 points

(a) 8 words of 6 bits (b) 16 words of 3 bits (c) 32 words of 6 bits (d) 64 words of 3 bits

(e) None of the above

Draw a block diagram of your memory with the major components, indicating its inputs and outputs.

Q8.

1) - Draw the state diagram of the sequential circuit whose state table is given below

The State Diagram goes here: 1.5 points

Present State A B C	Next state $A^+B^+C^+$	JA	KA	JB	KB	JC	KC
0 0 0	1 0 0						
0 0 1	1 1 0						
0 1 0	0 0 1						
1 0 0	0 1 0						
1 1 0	0 0 0						

- Fill out the above table with the appropriate values for the JK flip-flops inputs such that the sequential circuit will observe the required transitions. 1.5 points

- Indicate the correct set of minimized equations of the JK flip-flops inputs from the following: 2 points

(a) $\mathbf{J}_A = A'B'$, $\mathbf{K}_A = C'$, $\mathbf{J}_B = AB'C' + A'B'C$, $\mathbf{K}_B = BC'$, $\mathbf{J}_C = A'BC$ $\mathbf{K}_C = A'B'C$.

(b) $\mathbf{J}_A = A'B'$, $\mathbf{K}_A = 1$, $\mathbf{J}_B = A+C$, $\mathbf{K}_B = 1$, $\mathbf{J}_C = A'B$, $\mathbf{K}_C = 1$.

(c) $\mathbf{J}_A = B'$, $\mathbf{K}_A = 1$, $\mathbf{J}_B = A+C$, $\mathbf{K}_B = 1$, $\mathbf{J}_C = A'B$, $\mathbf{K}_C = 1$.

(d) $\mathbf{J}_A = A'B'$, $\mathbf{K}_A = A$, $\mathbf{J}_B = AC$, $\mathbf{K}_B = C'$, $\mathbf{J}_C = A'BC$, $\mathbf{K}_C = A'$.

(e) $\mathbf{J}_A = B'$, $\mathbf{K}_A = A$, $\mathbf{J}_B = AC$, $\mathbf{K}_B = C'$, $\mathbf{J}_C = A'BC$, $\mathbf{K}_C = A'$.

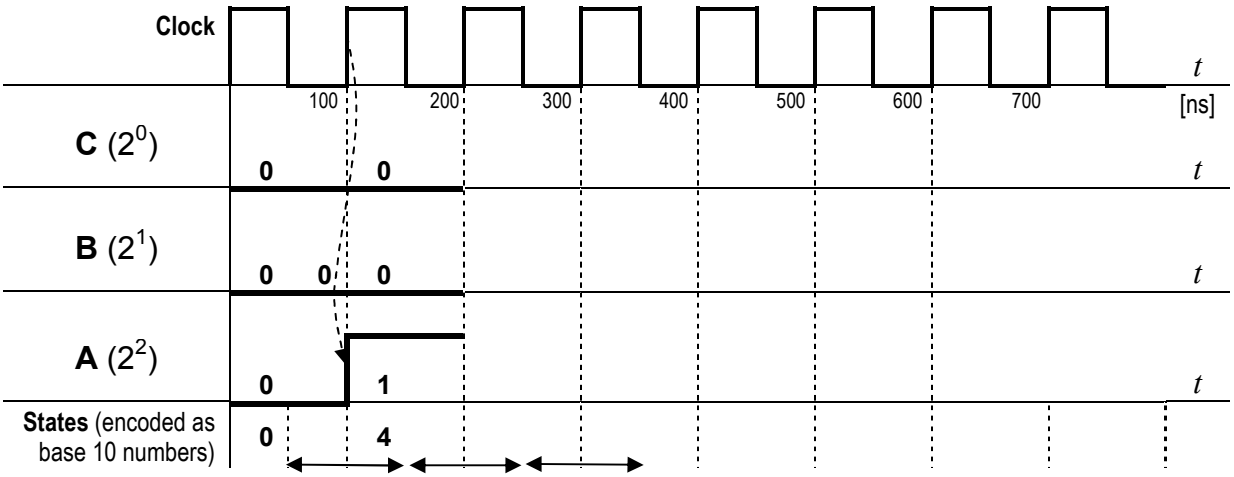
2) - If your circuit reaches by mistake any of the 3 states that are not used, determine their corresponding next state. 1.5 points

Present state	Next State

- Is your circuit auto-corrective? Reply just with YES or NO

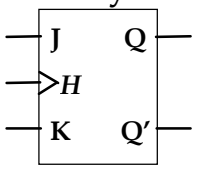
3) Draw the time diagram and give the states of the flip-flops' outputs through the first 6 clock pulses, assuming that their initial state (at t=0) is 000 and they are triggered on the rising edge of the clock.

1.5 points



Annex: JK flip-flop

Circuit symbol:



Characteristic Equation:

$$Q_{(t+1)} = JQ'_{(t)} + K'Q_{(t)}$$

Truth Table:

J	K	$Q_{(t+1)}$	
0	0	$Q_{(t)}$	No change
0	1	0	Q <- 0 (reset)
1	0	1	Q <- 1 (set)
1	1	$Q'_{(t)}$	Complement

Excitation Table

$Q_{(t)}$	$Q_{(t+1)}$	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

You can do your calculation here…
(to be submitted but will not be marked)

You can do your calculation here…
(to be submitted but will not be marked)

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(to be submitted but will not be marked)