ECSE 304-330

Introduction To Electronic Circuits

Midterm Examination
Tuesday March 13, 2012, 1:05 PM - 2:25 PM

Examiner: Prof. G. Roberts
Associate Examiner: none

Name: ____

Student No.:____________________________________

Instructions:

- Answer all 5 questions.
- Questions have equal weight; Distribution is indicated in brackets.
- Answer directly on the question sheet provided. You may use the back of the sheet to continue your answer.
- Only the sheets provided will be marked.
- This is a Closed-Book Exam;
- Write your name and student number on the top of this sheet; if pages are removed from the exam, write your name on the top of each of the question sheets that you want marked.
- Only the faculty-approved Standard Calculator is permitted.
- You are permitted Translation dictonaries ONLY.

Note To Student:

The instructor and / or his representative cannot and will not answer any questions during the final examination period. If you believe a question is in error or requires further clarification, please state your assumptions and work the problem from this point onwards. Clearly, if a question is in error, you will recieve full benefit.

Marking Scheme:

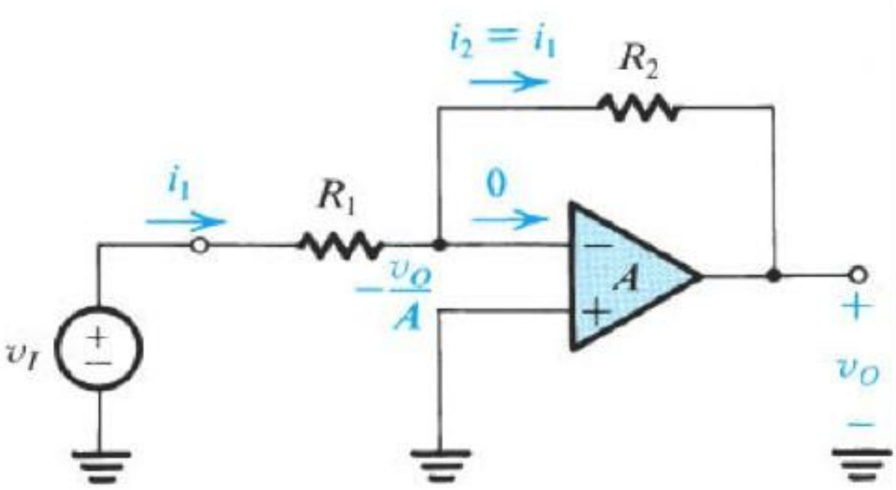
Q1 (10 points)	Q2 (10 points)	Q3 (10 points)	Q4 (10 points)	Q5 (10 points)	TOTAL

Question 1:

(a) Design an inverting amplifier that has a DC gain of maginitude greater than 50 V/V to connect to a transducer that generates a very weak signal. Assume that the op amp is ideal and the source resistance of the transducer is zero.

[2 points]

Solution



Given Data in Problem:

```
> restart:
> G_desired:=-50;
```

G_desired := K50 (1.1.1.1)

```
> A[op,desired]:=infinity;
```

$A_{op,\ desired}$:= N (1.1.1.2)

First step of the design process is to describe the input-output transfer function, G:

KCL at -ve input terminal of op amp:

```
> eqn1:=(v[I]-v[neg])/R[1]=(v[neg]-v[o])/R[2];
```

$$eqn1 := \frac{v_I \text{ K } v_{neg}}{R_1} = \frac{v_{neg} \text{ K } v_o}{R_2} \quad (1.1.1.3)$$

Now, the op amp input-output behavior can be described as

```
> v[neg]:=-v[o]/A[op];
```

$$v_{neg} := \text{K} \frac{v_o}{A_{op}} \quad (1.1.1.4)$$

Solving for the output, we get

```
> v[o]:=solve(eqn1, v[o]);
```

(1.1.1.5)

$$v_o := K \frac{v_I A_{op} R_2}{R_1 C A_{op} R_1 C R_2} \tag{1.1.1.5}$$

Now imposing the ideal op amp condition, i.e. A_{op} =infinity, we write

> v[o]:=limit(v[o], A[op]=infinity, left);

$$v_o := K \frac{v_I R_2}{R_1} \tag{1.1.1.6}$$

> G:=v[o]/v[I];

$$G := K \frac{R_2}{R_1} \tag{1.1.1.7}$$

In order to satisfy the design requirements, G=-50 V/V, we see that we have one degrees of design freedom, i.e.

> G=G_desired;

$$K=K50 \frac{R_2}{R_1} \tag{1.1.1.8}$$

Let R_1 =1 kΩ, then we solve for R_2 according to

> R[1]:=1000:

> R[2]:=solve(G=G_desired, R[2]);

$$R_2 := 50000 \tag{1.1.1.9}$$

Therefore we select R_1 = 1 kΩ and R_2 = 50 kΩ.

(b) A transducer is found to have a source resistance of 100 kW. Modify the amplifier you designed in part (a) such that the input resistance to the inverting amplifier is no less than 200 kW. Provide details supporting your claim.

[2 points]

Solution

Given Data in Problem:

```
> G_desired:=-50;
```

$$G\_desired := K50 \quad (1.2.1.1)$$

```
> A[op,desired]:=infinity;
```

$$A_{op,\ desired} := N \quad (1.2.1.2)$$

```
> R[IN]>=200e3;
```

$$2.00\ 10^5 \% R_{IN} \quad (1.2.1.3)$$

Reset parameters from part (a)

```
> R[1]:='R[1]': R[2]:='R[2]':
```

As the value of R_1 is determined by the input resistance of the amplifier, we write

```
> R[1]:=R[IN];
```

$$R_1 := R_{IN} \quad (1.2.1.4)$$

We must augment the design of part (a) by adding the above new constraint as follows:

```
> 'G'=G;
```

$$G = K\frac{R_2}{R_{IN}} \quad (1.2.1.5)$$

```
> R[IN]:=200e3;
```

$$R_{IN} := 2.00\ 10^5 \quad (1.2.1.6)$$

```
> R[1]:=R[IN];
> R[2]:=solve(G=G_desired, R[2]);
```

$$R_1 := 2.00\ 10^5$$

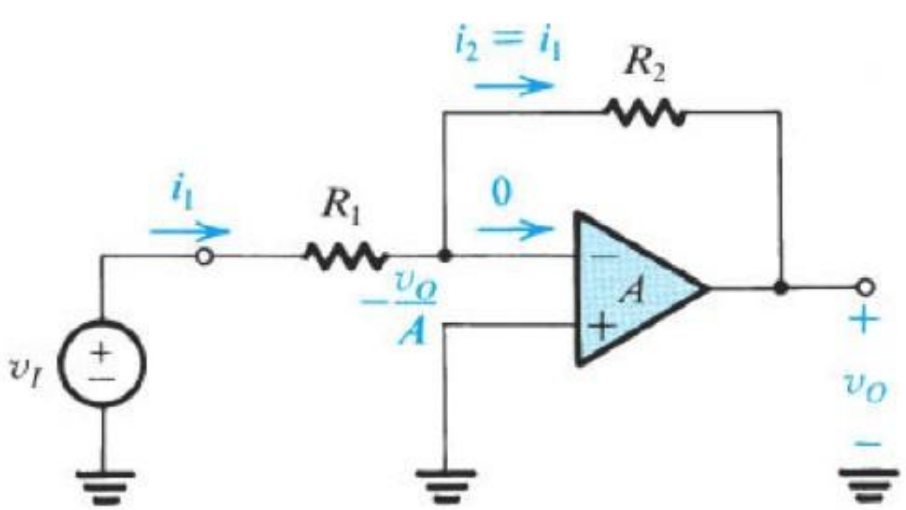
$$R_2 := 1.0000000\ 10^7 \quad (1.2.1.7)$$

Therefore we select R_1 = 200 kΩ and R_2 = 10 MΩ.

(c) What is the unity-gain frequency requirements of an op amp that is used in an inverting amplifier with a DC gain of magnitude greater than or equal to 50 V/V and having a 3-dB bandwidth of at least 2,000 rad/s.

[5 points]

Solution




```
> restart:                #clear memory
```

In part (a), we derived the output voltage in terms of the input signal and parameters of the circuit, including the op amp gain. Repeating here we write:

```
> v[o] := -v[I]*A[op]*R[2]/(R[2]+R[1]+A[op]*R[1]);
```

$$v_o := K \frac{v_I A_{op} R_2}{R_2 \, C \, R_1 \, C \, A_{op} R_1} \quad (1.3.1.1)$$

```
> G:=v[o]/v[I];
```

$$G := K \frac{A_{op} R_2}{R_2 \, C \, R_1 \, C \, A_{op} R_1} \quad (1.3.1.2)$$

Now assume the op amp is modeled with a single pole transfer function, we write

```
> A[op]:=A[o]/(1+s/omega[b]);
```

$$A_{op} := (1.3.1.3) \; \frac{A_o}{1C \, \frac{s}{wb}}$$

```
> G:=normal(G);
```

$$G := K \frac{R_2 \, wb \, A_o}{R_2 \, wb \, C \, R_2 \, s \, C \, R_1 \, wb \, C \, R_1 \, s \, C \, A_o \, wb \, R_1} \quad (1.3.1.4)$$

```
> N:=numer(G):
```

```
> P:=collect(denom(G),s):
> LCp:=coeff(P,s,0):
> G:=normal(N/LCp)/collect(P/LCp,s);;
```

$$G := K\frac{R_2\,A_o}{\left(R_2\,C\,R_1\,C\,A_o\,R_1 1 C\right)\left(\dfrac{R_2\,C\,R_1\,s}{R_2\,w_b\,C\,R_1\,w_b\,C\,A_o\,w_b\,R_1}\right)} \qquad (1.3.1.5)$$

Here we see the DC gain and 3-dB bandwidth (root of the characteristic equation) is described as follows:

```
> A[DC,CL]:=eval(G,s=0);
```

$$A_{DC,\,CL} := K\frac{R_2\,A_o}{R_2\,C\,R_1\,C\,A_o\,R_1} \qquad (1.3.1.6)$$

or we can write

```
> A[DC, CL] := -R[2]/R[1]*A[o]/(1+R[2]/R[1]+A[o]);
```

$$A_{DC,\,CL} := K\frac{R_2\,A_o}{R_1\,1\,C\,C\,A_o\left(\dfrac{R_2}{R_1}\right)} \qquad (1.3.1.7)$$

and recongize that $A_o >> 1 + R_2/R_1$, we can approximate the above expression as

```
> A[DC, CL] := -R[2]/R[1]*A[o]/(A[o]);
```

$$A_{DC,\,CL} := K\frac{R_2}{R_1} \qquad (1.3.1.8)$$

Likewide the 3-dB bandwidth can be written as

```
> omega[3-dB,CL]:=-1*solve(denom(G)=0,s);
```

$$w_{3\,K\,dB,\,CL} := \frac{\left(R_2\,C\,R_1\,C\,A_o\,R_1\right)w_b}{R_2\,C\,R_1} \qquad (1.3.1.9)$$

which can be further simplified by imposing the condition, $A_o >> 1 + R_2/R_1$, leading to

```
> omega[3-dB, CL] := (A[o]*R[1])*omega[b]/(R[2]+R[1]);
```

$$w_{3\,K\,dB,\,CL} := \frac{A_o\,R_1\,w_b}{R_2\,C\,R_1} \qquad (1.3.1.10)$$

Now, the op amp unioty-gain bandwidth is given by

```
> omega[t]=A[o]*omega[b];
```

$$w_t = w_b\,A_o \qquad (1.3.1.11)$$

which allows us to write the closed-loop bandwidth as

```
> omega[3-dB, CL]:=subs(omega[b]=omega[t]/A[o], omega[3-dB,
  CL] );
```

$$w_{3\,K\,dB,\,CL} := \frac{R_1\,w_t}{R_2\,C\,R_1} \qquad (1.3.1.12)$$

Substituting our known circuit information (found from part (a) above):

```
> R[1]:=1e3: R[2]:=50e3:
```

We see the DC gain and 3-dB bandwidth become

```
> A[DC,CL];
```

$$-50.00000000 \quad (1.3.1.13)$$

```
> omega[3-dB,CL];
```

$$0.01960784314\ \omega_t \quad (1.3.1.14)$$

Now our design requirements are

```
> 'omega[3-dB,CL]' >= 2e3;
```

$$2000. \le \omega_{3-dB,\ CL} \quad (1.3.1.15)$$

leading to the following set of equations

```
> omega[3-dB,CL] >= 2e3;
```

$$2000. \le 0.01960784314\ \omega_t \quad (1.3.1.16)$$

Solving for the above specific condition, we write

```
> omega[t]=solve(omega[3-dB,CL] = 2e3, omega[t]);
```

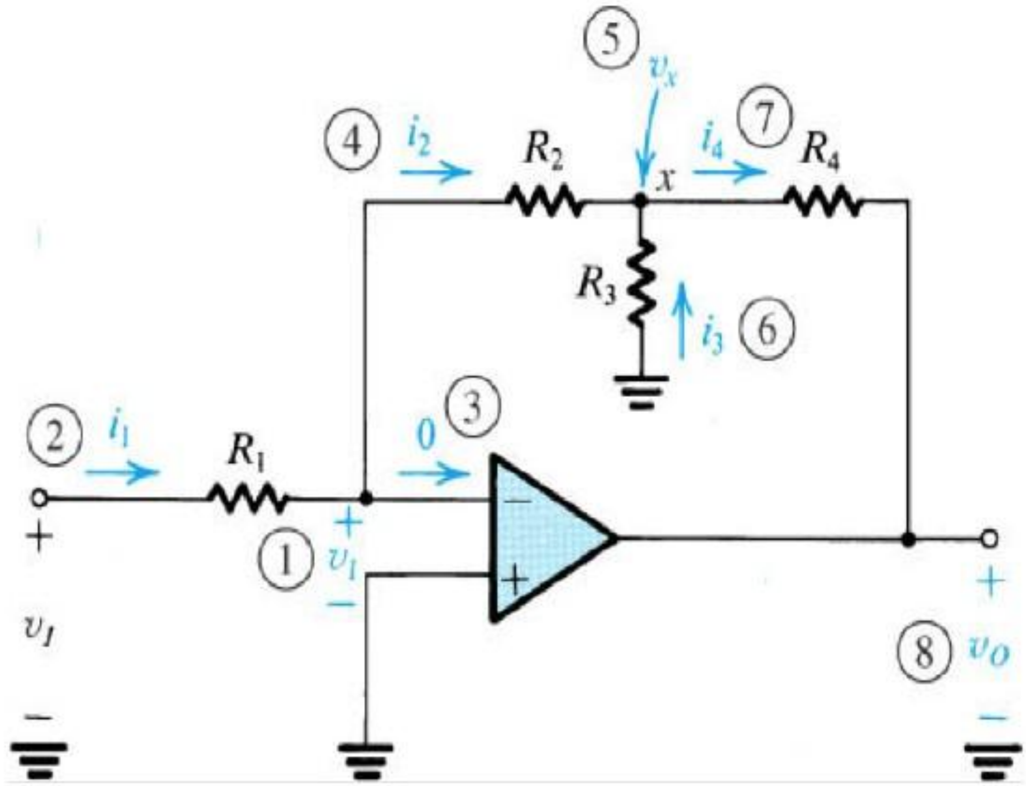
$$\omega_t = 1.020000000\ 10^5 \quad (1.3.1.17)$$

Therefore the op amp needs a unity-gain bandwidth slightly larger than 100 kHz.

(d) If the minimum required input resistance to the amplifier was increased to 1 MW, suggest a method in which to realize the amplifier using resistors with values no greater than 10 MW. No component calculations are required, just a circuit diagram.

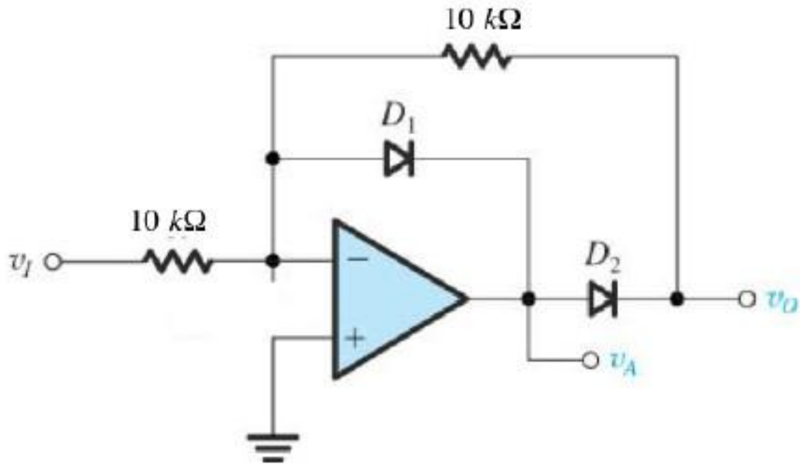
[1 points]

Solution



Question 2:

The transient operation of the nonlinear circuit shown below is to be verified using Spice. Using the Spice summary sheet found at the end of this exam, answer the following questions.

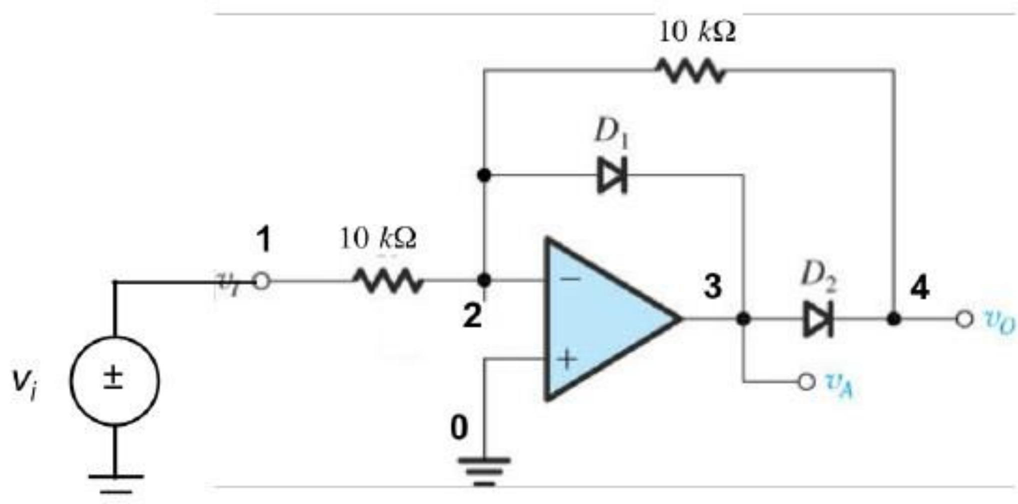


(a) Identify the nodes on the above schematic that will be used by Spice to perform analysis.

[1 points]

Solution

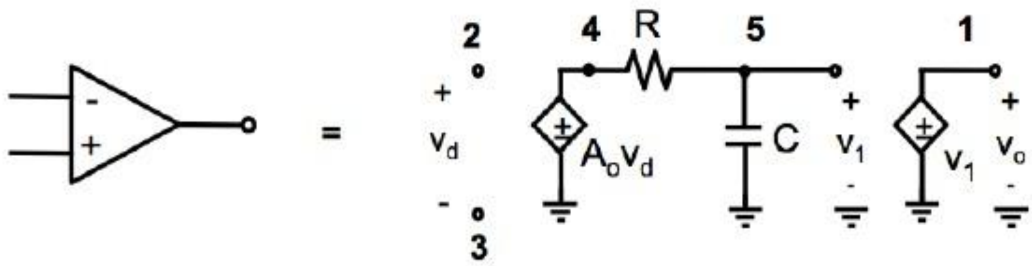
Circuit that is to be simulated with transistent source added:



(b) Describe the model of the op amp you would use to simulate the frequency dependent behavior of the op amp having a 3-dB bandwidth of 100 rad/s and a DC gain of 10,000 V/V.

[3 points]

Solution



> restart:

For a DC gain of 10,000 V/V, we set

> Ao:=10e3;

Ao := 10000. (2.2.1.1)

Establishing the op amp parameters for a 3 db bandwidth of 100 rad/s, we solve for R, assuming C is 1 uF as follows:

> wb:=100;

wb := 100 (2.2.1.2)

> C:=1e-6;

C := 0.000001 (2.2.1.3)

> R:=solve(wb=1/(R*C), R);

R := 10000. (2.2.1.4)

(c) If the two diodes are asumed to have $I_S=10^{-14}$ A and η=1.2 write the SPICE statements that are used to describe D_1 and D_2 .

[2 points]

Solution

```
D1 2 3 diode
D2 3 4 diode
.model diode D ( Is=1e-14 n=1.0 )
```

(d) Write a Spice netlist that describes your circuit, including the input stimulus, the analysis statement and the print/plot or probe statement.

[4 points]

PSpice Netlist

Nonlinear Diode Circuit

```
* op-amp subcircuit
.subckt small_signal_opamp 1 2 3
* connections:| | |
*output | |
*+ve input |
*-ve input
E1 4 0 2 3 1e4
R 4 5 1e4
C 5 0 1e-6
Eoutput 1 0 5 0 1
.ends small_signal_opamp


** Main Circuit **
* signal source
Vi 1 0 PULSE (0V 1V 0s 1us 1us 0.5ms 1ms)
```

```
Xopamp 3 0 2 small_signal_opamp
R1 1 2 10k
R2 2 4 10k
D1 2 3 diode
D2 3 4 diode
.model diode D ( Is=1e-14 n=1.0 )
** Analysis Requests **
.TRAN 10us 3ms 0ms 10us
** Output Requests **
.PRINT TRAN V(4) V(1)
.probe
.end
```

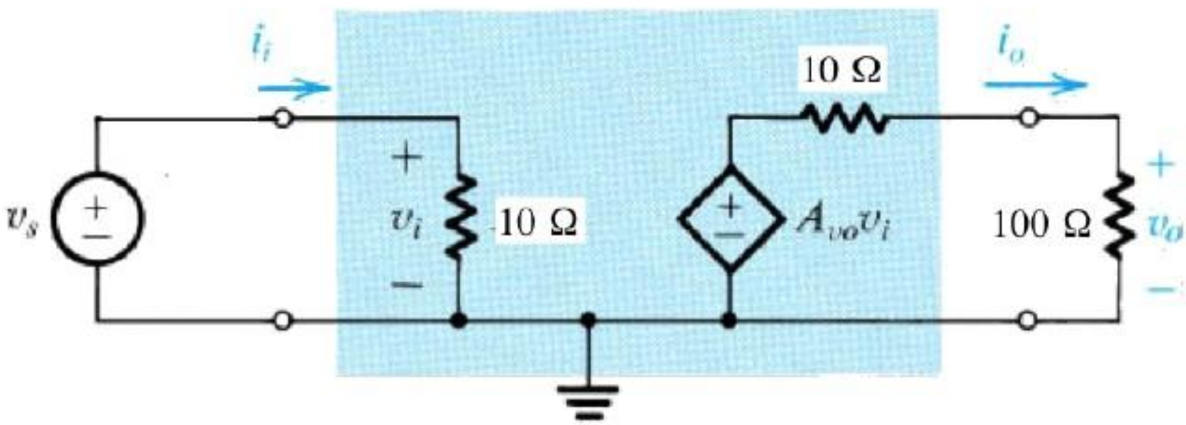
Question 3:

An amplifier with 40 dB of small-signal, open-circuit voltage gain, an input resistance of 10 Ω, and an output resistance of 10 Ω, drives a load of 100 Ω.

(a) What voltage and power gains (expressed in dB) would you expect with the load connected?

[5 points]

Solution:



Amplifier Configuration

Given Data in Problem:

```
> restart:
> A[vo,dB]:=40:
> Ri:=10: Ro:=10: Rl:=100:
```

Input voltage

```
> vi:=vs:
```

No-load voltage gain of amplifier in V/V

```
> Avo:=10^(A[vo,dB]/20);
```

$$Avo := 100 \quad (3.1.1.1)$$

Solving for the output voltage, we write

```
> v[o,loaded]:=Avo*vi*Rl/(Rl+Ro);
```

$$v_{o,\,loaded} := \frac{1000\, vs}{11} \quad (3.1.1.2)$$

The voltage gain in V/V and dB is therefore

```
> A[v,loaded]:=v[o,loaded]/vs;
> A[v,loaded,dB]:=evalf[3](20*log10(A[v,loaded]));
```

$$A_{v,\,loaded} := \frac{1000}{11}$$

(3.1.1.3)

$$A_{v,\ loaded,\ dB} := 39.2 \tag{3.1.1.3}$$

As the input and output power is

```
> P[i]:=vi^2/Ri;
```

$$P_i := \frac{1}{10} vs^2 \tag{3.1.1.4}$$

```
> P[o]:=v[o,loaded]^2/Rl;
```

$$P_o := \frac{10000}{121} vs^2 \tag{3.1.1.5}$$

The power gain in W/W and dB is

```
> A[p,loaded]:=evalf(P[o]/P[i]);
> A[p,loaded,dB]:=evalf[3](10*log10(A[p,loaded]));
```

$$A_{p,\ loaded} := 826.4462810$$

$$A_{p,\ loaded,\ dB} := 29.2 \tag{3.1.1.6}$$

The voltage gain in dB is 39.2 dB and the power gain is 29.2 dB.

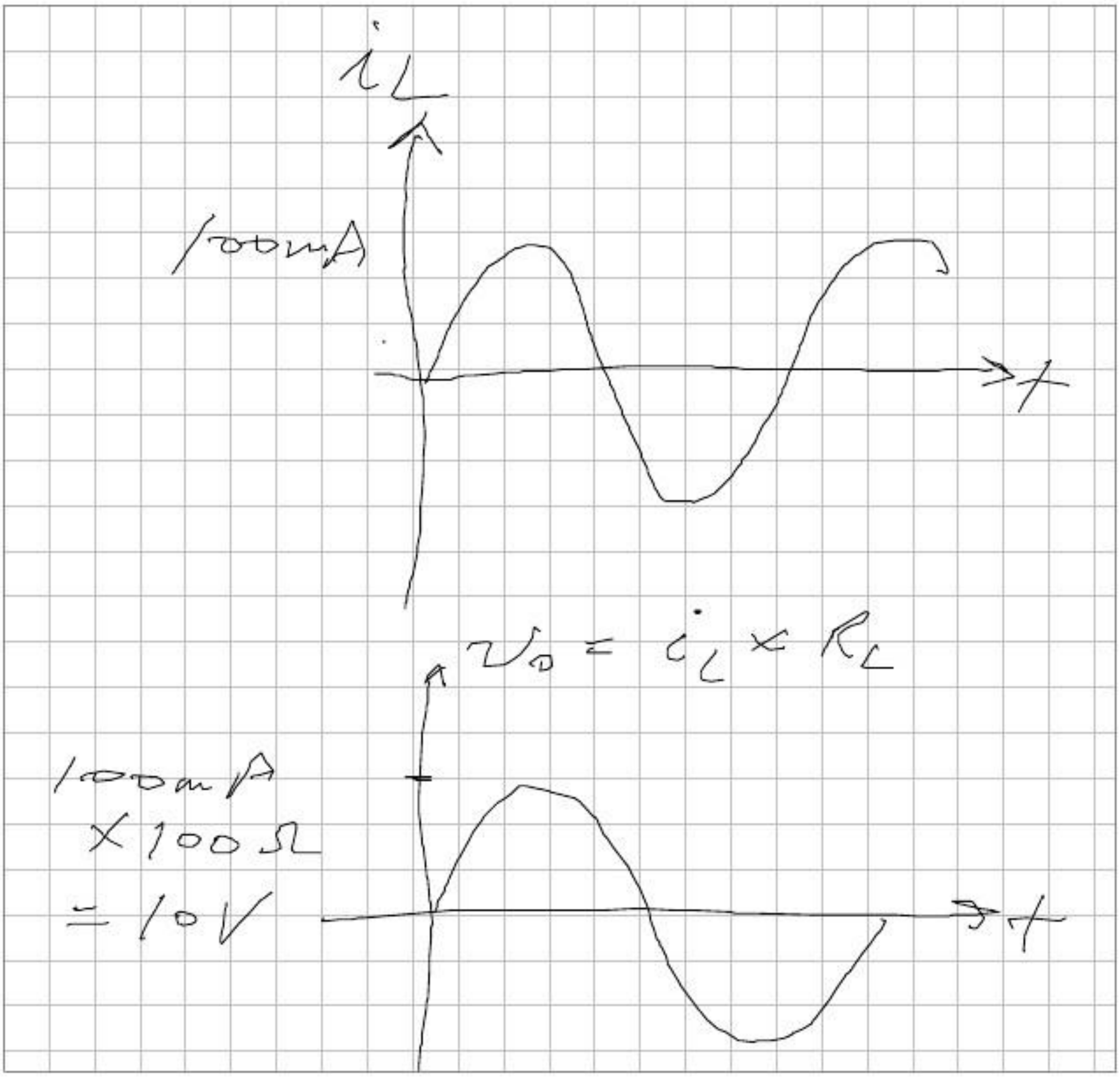
(b) If the amplifier has a peak output-current limitation of 100 mA, what is the value of the largest sine-wave input for which undistorted output is possible? What is the corresponding output power available?

[5 points]

Solution

Given data

```
> i[load,peak]:=100e-3: Rl:=100:
```



The output voltage in V is

```
> v[o,peak]:=i[load,peak]*Rl;
```

$$v_{o,\,peak} := 10.000 \quad (3.2.1.1)$$

The corresponding input signal is

```
> v[input,peak]:=v[o,peak]/A[v,loaded];
```

$$v_{input,\,peak} := 0.1100000000 \qquad (3.2.1.2)$$

The output power in W under peak conditions is

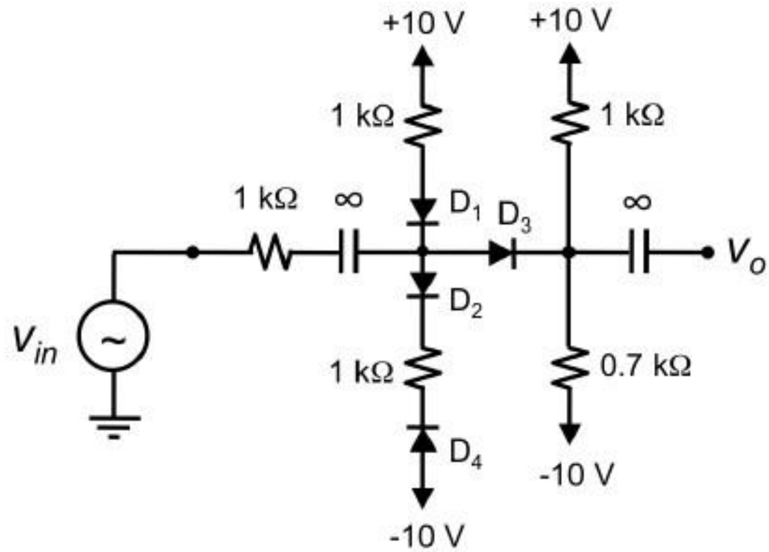
```
> P[o,peak]:=evalf[3]((v[o,peak]/sqrt(2))^2/Rl);
```

$$P_{o,\,peak} := 0.500 \qquad (3.2.1.3)$$

For a peak output voltage of 10 V requires a peak input voltage of 110 mV; The corresponding output power is 0.5 W.

Question 4:

For the diode circuit shown to the right, answer the following questions.The capacitors are assumed to have no affect on AC signals only DC signals.

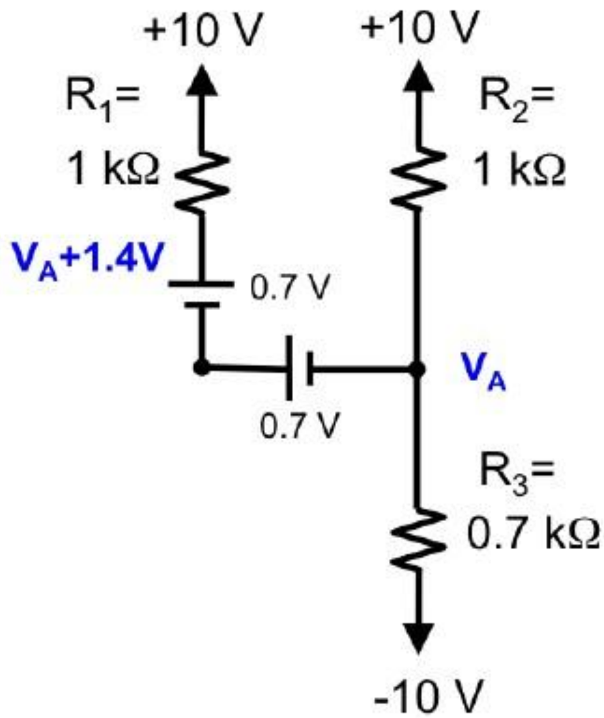


(a) Assuming a 0.7 V drop model for each diode, determine the bias current through each diode. Determine which diodes are OFF and which are ON.

[4 points]

Solution:

Assuming D2 and D4 is OFF, and D2 and D3 are ON, calculate the diode currents according to the following schematic:



> restart:

Data for problem:

> R1:=1e3: R2:=1e3: R3:=700: Vdd:=10: Vss:=-10:

Solving for the center node voltage VA, we write KCL as follows:

> eqn:=(Vdd-(VA+1.4))/R1+(Vdd-VA)/R2 - (VA-Vss)/R3=0;

eqn := 0.00431428571 K 0.003428571429 VA = 0 (4.1.1)

> VA:=solve(eqn,VA);

VA := 1.258333332 (4.1.2)

> #VA:=1:

> #R3:=solve(eqn,R3);

Solve for the branch currents (must all be positive or else assumption is wrong):

> i[D1]:=(10-VA-1.4)/R1;

> i[D2]:=0;

> i[D3]:=i[D1];

> i[D4]:=0;

i_{D1} := 0.007341666668

i_{D2} := 0

i_{D3} := 0.007341666668

i_{D4} := 0 (4.1.3)

Solve for the branch currents (must all be positive or else assumption is wrong):

> I1:=(Vdd-(VA+1.4))/R1;

> I2:=(Vdd-VA)/R2;

> I3:=(VA-Vss)/R3;

I1 := 0.007341666668

I2 := 0.008741666668

(4.1.4)

$$I3 := 0.01608333333 \tag{4.1.4}$$

As all currents are positive, our assumptions about each diode is correct.

(b) Assuming each diode has a small-signal resistance defined according to

$$r_D = \frac{nV_T}{I_D}$$

draw the small-signal equivalent circuit. Quantify all diode resistances in your schematic assuming η=1.

[3 points]

Solution:

Device Parameters:

```
> n:=1: V[T]:=25e-3:
```

Let us calculate the small-signal resistance of each diode that is forward biased. Diodes that are reversed biased have infinite incremental resistance.

```
> r[D1]:=n*V[T]/i[D1];
```

$$r_{D1} := 3.405221339 \quad (4.2.1)$$

```
> r[D2]:=infinity;
```

$$r_{D2} := N \quad (4.2.2)$$

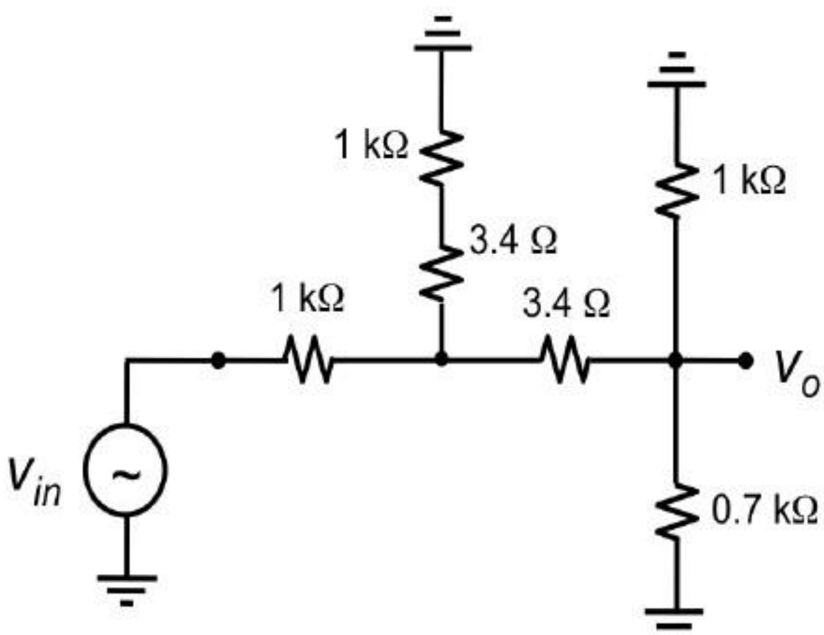
```
> r[D3]:=n*V[T]/i[D3];
```

$$r_{D3} := 3.405221339 \quad (4.2.3)$$

```
> r[D4]:=infinity;
```

$$r_{D4} := N \quad (4.2.4)$$

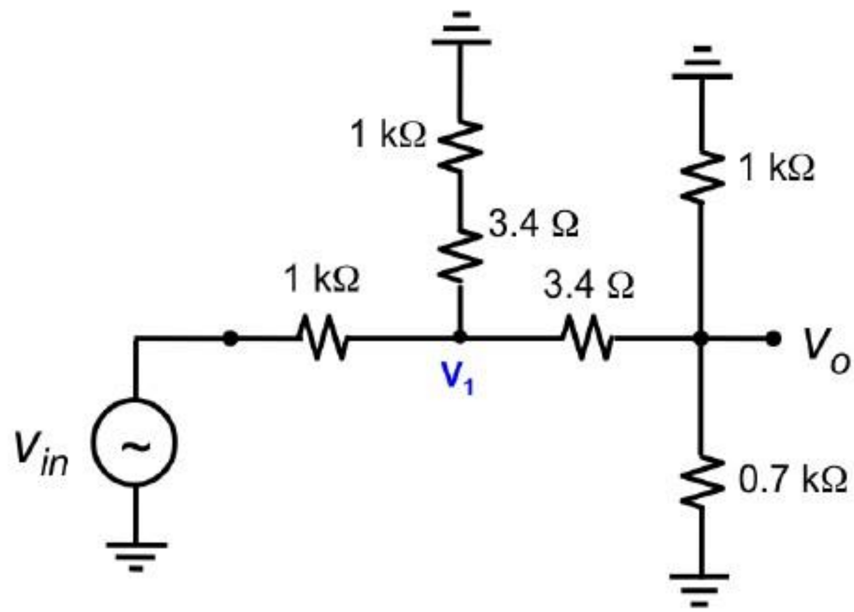
The small-signal equivalent circuit becomes



(c) What is the small-signal voltage gain Vo/Vin.

[3 points]

Solution:
Using the small-signal equivalent circuit,



we write two KCL eqns and solve for the output voltage:

```
> eqn1:= (vin-v1)/1e3 + (0-v1)/(1e3+3.4) + (vo-v1)/3.4 = 0:
> eqn2:= (v1-vo)/3.4 + (0-vo)/1e3 + (vo-0)/700 = 0:
> sol:=solve({eqn1,eqn2}, [v1, vo]);
```

sol := [[v1 = 0.6379932513 vin, vo = 0.6389242552 vin]] (4.3.1)

```
> assign(sol);
```

Finally, expressing the output in terms of the input signal we write

```
> 'vo'=vo;
```

vo = 0.6389242552 vin (4.3.2)

The small-signal gain then becomes

```
> G:=vo/vin;
```

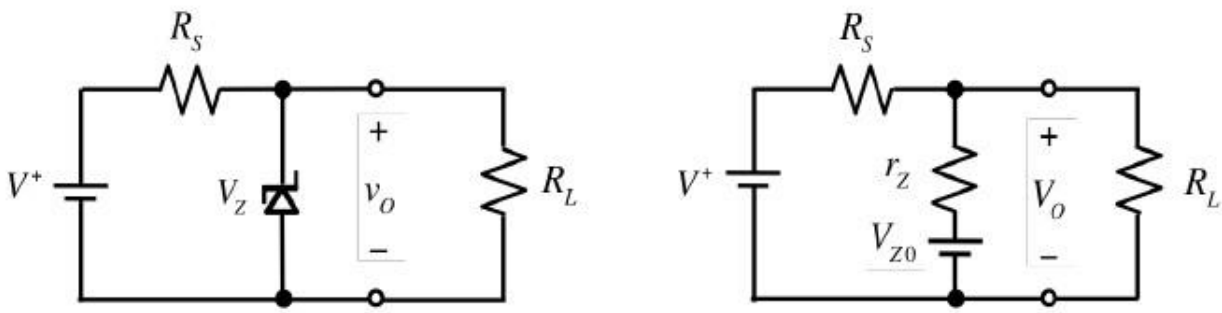
G := 0.6389242552 (4.3.3)

Question 5:

Design an 8.0 V zener regulator circuit using a 8.0 V zener diode specified at 10 mA. The zener has an incremental resistance r_z = 30 Ω and a knee current of 0.5 mA. The regulator operates from a 12-V supply and has a 1.2-kΩ load. Once the design is complete answer the following questions.

(a) Place Design Details Here:

[4 points]




```
> restart:
```

Given Information:

```
> Vp:=12: Vz:=8.0: Iz:=10e-3: Izk:=0.5e-3: rz:=30: Rl:=1.2e3:
```

The design problem is to find the value of Rs once the zener diode parameters are established.

```
> Vz0:=Vz-rz*Iz;
```

$$Vz0 := 7.700 \quad (5.1.1)$$

Load current conditions:

```
> # set the maximum load current at least twice the nominal
   current level:
> i[load,nominal]:=8.0/Rl;
> i[load,max]:=20e-3;
> if i[load,max] > i[load,nominal] then printf("¥t¥t¥t¥t¥t
   load current condition is met") else printf("¥t¥t¥t¥t¥t load
   current condition is NOT met") end if;
> i['Rs',max]:=i[load,max]+Izk;
```

$$i_{load,\ nominal} := 0.006666666666$$

```
!!!!!
 load current condition is met
```

$$i_{Rs,\ max} := 0.0205 \quad (5.1.2)$$

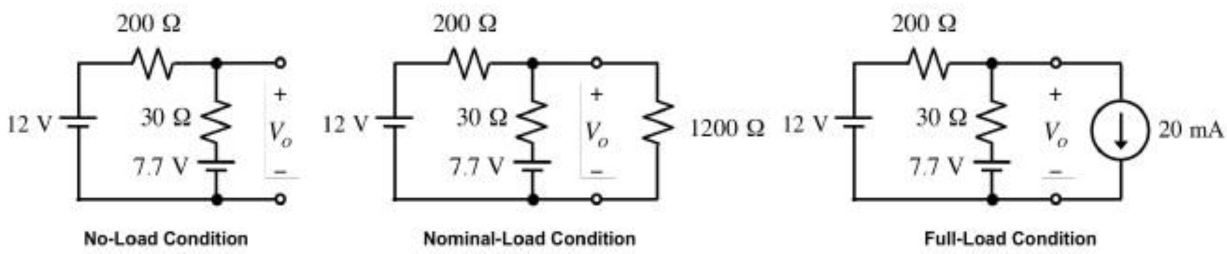
Series resistor Computation:

```
> Rs_nominal:=(Vp-Vz0-i['Rs',max]*rz)/i['Rs',max];
> # based on the above results, select Rs slightly larger, i.e.,
> Rs:=200;
```

$$Rs\_nominal := 179.7560976$$

$$Rs := 200 \quad (5.1.3)$$

Select Rs equal to 200 ohms resulting in the following equivalent circuits:



Check the output voltage at no-load using KCL:

```
> eqn:= (12-Vo)/200 + (7.7-Vo)/30 = 0:
> v[o,noload]:=solve(eqn,Vo); i[z,noload]:=(v[o,noload]-7.7)/rz;
  i[o,noload]:=0;
```

$$v_{o,\ noload} := 8.260869566$$

$$i_{z,\ noload} := 0.01869565220$$

$$i_{o,\ noload} := 0 \tag{5.1.4}$$

Check the output voltage at 1200 ohm load using KCL:

```
> eqn:= (12-Vo)/200 + (7.7-Vo)/30 - Vo/1200 = 0:
> v[o,nominalload]:=solve(eqn,Vo); i[z,nominalload]:=(v[o,
  nominalload]-7.7)/rz; i[o,nominalload]:=v[o,nominalload]/Rl;
```

$$v_{o,\ nominalload} := 8.085106384$$

$$i_{z,\ nominalload} := 0.01283687947$$

$$i_{o,\ nominalload} := 0.006737588653 \tag{5.1.5}$$

Check the output voltage at maximum load using KCL:

```
> eqn:= (12-Vo)/200 + (7.7-Vo)/30 - 20e-3 = 0:
> v[o,maxload]:=solve(eqn,Vo); i[z,maxload]:=(v[o,maxload]-7.7)
  /rz; i[o,maxload]:=20e-3; test: i[z,maxload] > Izk;
```

$$v_{o,\ maxload} := 7.739130436$$

$$i_{z,\ maxload} := 0.001304347867$$

$$i_{o,\ maxload} := 0.020$$

$$0.0005 \ ! \ 0.001304347867 \tag{5.1.6}$$

(b) What is the value of the series zener resistor used in your design?

[1 points]

> Rs:=200;

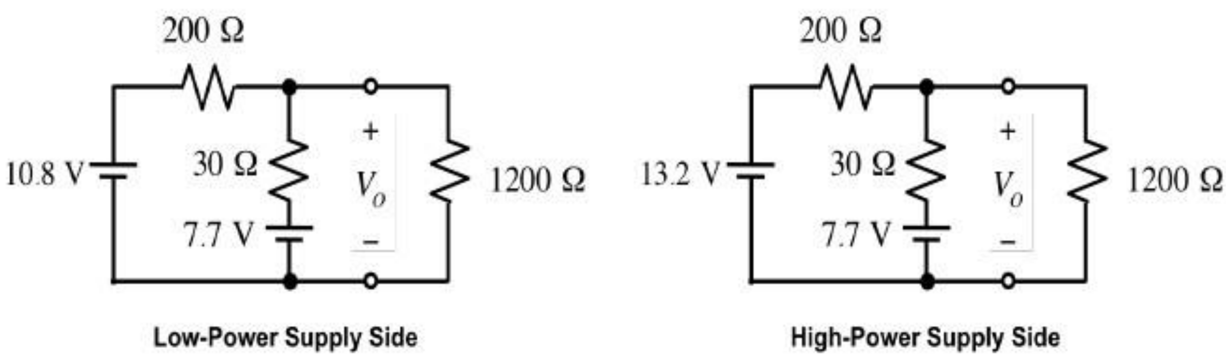
$$Rs := 200 \tag{5.2.1}$$

The series resistor is equal to 200 ohms.

(c) What is the regulator output voltage when the supply is 10% high? What about if it is 10% low? Assume the regulator remains loaded with the 1200 ohm load.

[2 points]

Circuit problem:



> restart:

Output Voltage Under Low-Power Supply

> Vp:=12: Vz:=8.0: Rs:=200: rz:=30: Rl:=1200:
> Rlp:=1/(1/Rl+1/rz):
> # small-signal approximation
> v[o,delta,LPS]:= Rlp/(Rs+Rlp)*(-0.1*Vp);

$$v_{o,\,d,\,LPS} := \text{K}0.1531914894 \tag{5.3.1}$$

> v[o,LPS]:=Vz+v[o,delta,LPS];

$$v_{o,\,LPS} := 7.846808511 \tag{5.3.2}$$

Output Voltage Under High-Power Supply

> # small-signal approximation
> v[o,delta,HPS]:= Rlp/(Rs+Rlp)*(+0.1*Vp);

$$v_{o,\,d,\,HPS} := 0.1531914894 \tag{5.3.3}$$

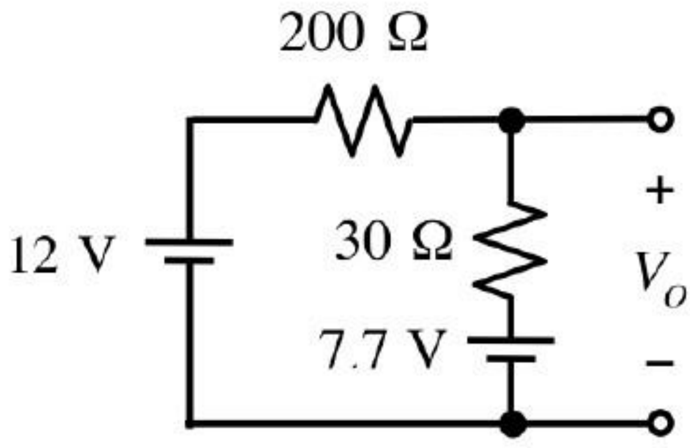
> v[o,HPS]:=Vz+v[o,delta,HPS];

$$v_{o,\,HPS} := 8.153191489 \tag{5.3.4}$$

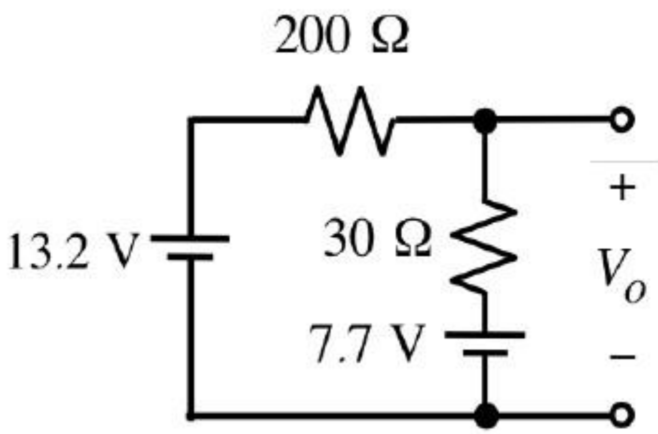
The output voltage varies from 7.84 V to 8.15 V for a power supply variation from 10.8 V to 13.2 V.

(d) What is the regulator output voltage when both the supply is 10% high and the load is removed?

[1 points]
Circuit problem:



Nominal Power Supply Side, No Load



High-Power Supply Side, No Load

Output Voltage Under High-Power Supply, No Load Conditions

```
> eqn1:= (12-Vo)/200 + (7.7-Vo)/30 = 0:
> v[o,noload]:=solve(eqn1,Vo);
```

$$v_{o,\ noload} := 8.260869566 \quad (5.4.1)$$

```
> v[o,noload,delta,HPS]:= rz/(Rs+rz)*(+0.1*Vp);
```

$$v_{o,\ noload,\ d,\ HPS} := 0.1565217391 \quad (5.4.2)$$

```
> v[o,noload,HPS]:=v[o,noload]+v[o,noload,delta,HPS];
```

$$v_{o,\ noload,\ HPS} := 8.417391305 \quad (5.4.3)$$

```
> # compare with direct calculation
> eqn2:= (13.2-Vo)/200 + (7.7-Vo)/30 = 0:
```

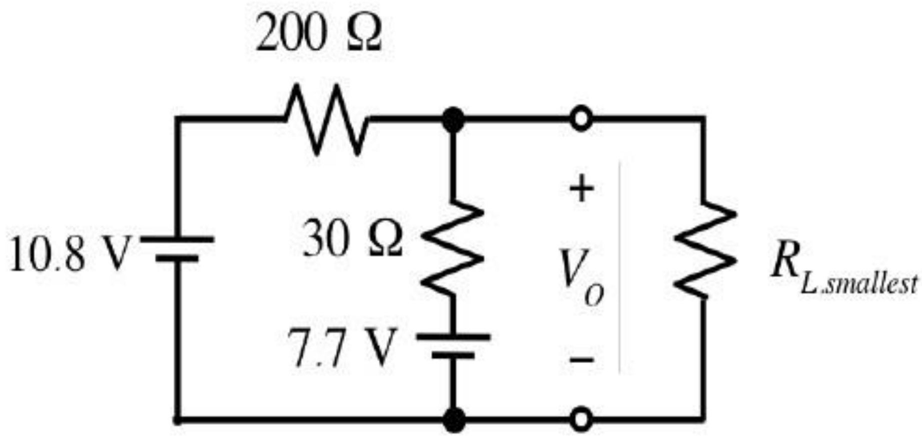
```
> v[o,noload,HPS]:=solve(eqn2,Vo);
```

$$v_{o,\,noload,\,HPS} := 8.417391305 \tag{5.4.4}$$

The no-load output voltage is approximately 8.42 V.

(e) What is the smallest possible load resistor that can be used while the zener operates at a current no lower than the knee current while the supply is 10% low? What is the load voltage in this case?

[2 points]
Circuit problem:




```
> restart:
```

Given Information:

```
> Vp:=12: Vz:=8.0: Iz:=10e-3: Izk:=0.5e-3: rz:=30: Rl:=1.2e3:
```

Maximum load conditions with a knee current of 0.5 mA

```
> Vz0:=Vz-rz*Iz;
```

$$Vz0 := 7.700 \quad (5.5.1)$$

```
> v[o,minimum]:=Vz0+rz*Izk;
```

$$v_{o,\,minimum} := 7.7150 \quad (5.5.2)$$

```
> eqn:= (12-Vo)/200 + (7.7-Vo)/30 - Vo/R[L,smallest] = 0;
> Vo:=v[o,minimum];
```

$$eqn := 0.3166666667 - \frac{23 Vo}{600} - \frac{Vo}{R_{L,\,smallest}} = 0$$

$$Vo := 7.7150 \quad (5.5.3)$$

```
> R[L,smallest]:=solve(eqn,R[L,smallest]);
```

$$R_{L,\,smallest} := 368.6977300 \quad (5.5.4)$$

```
> i[L,maximum]:=v[o,minimum]/R[L,smallest];
```

$$i_{L,\,maximum} := 0.02092500000 \quad (5.5.5)$$

The smallest load resistance is 369 Ω corresponding to a maximum load current of 20.0 mA.
The minimum load voltage is 7.72 V.